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SEPT 14

Issue 19/2006

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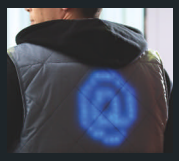

MAKING WAVES

Eight years later, details still matter

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SDR GOES TO WAR

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ABRACADABRA: MAKING SYSTEM INTERCONNECT DISAPPEAR WITH FPGAs

Page 59

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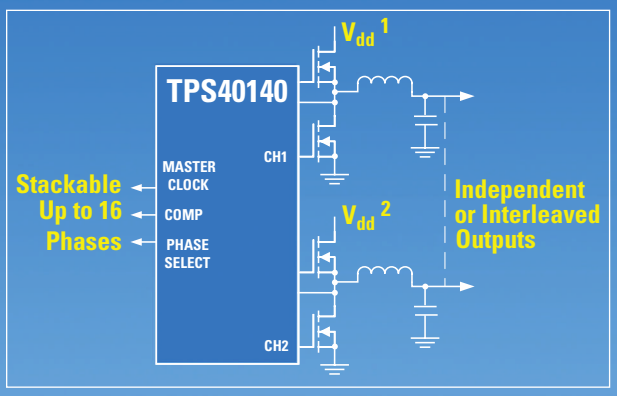

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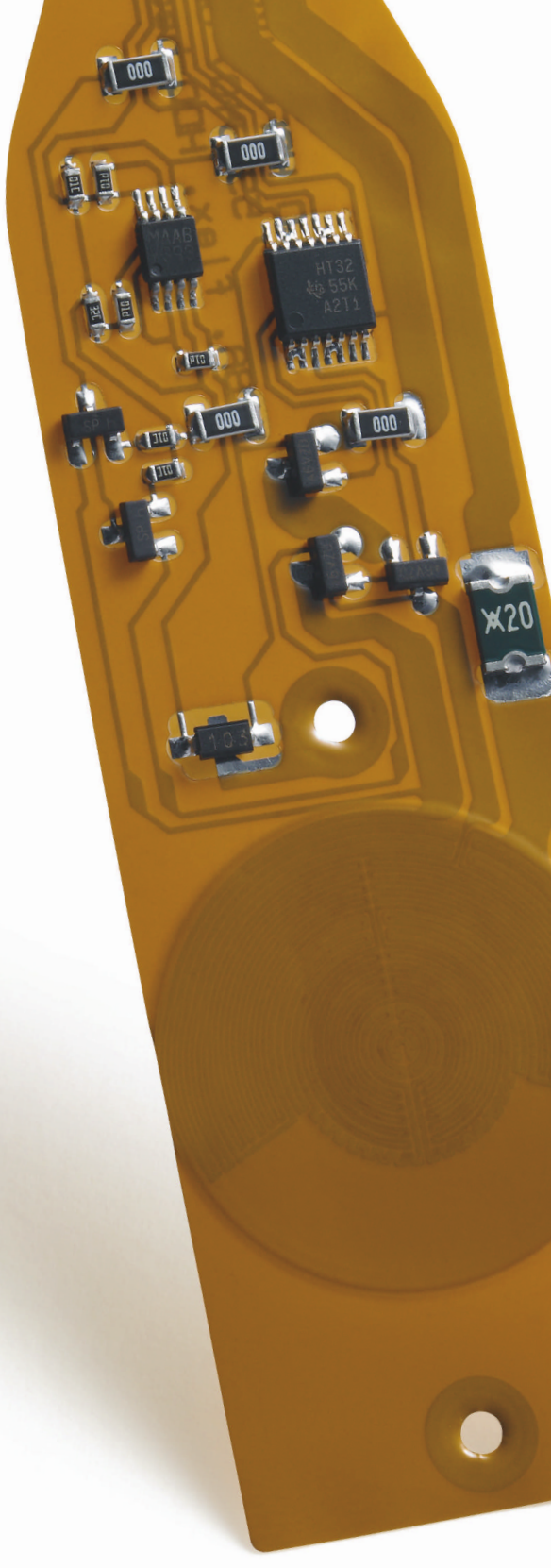

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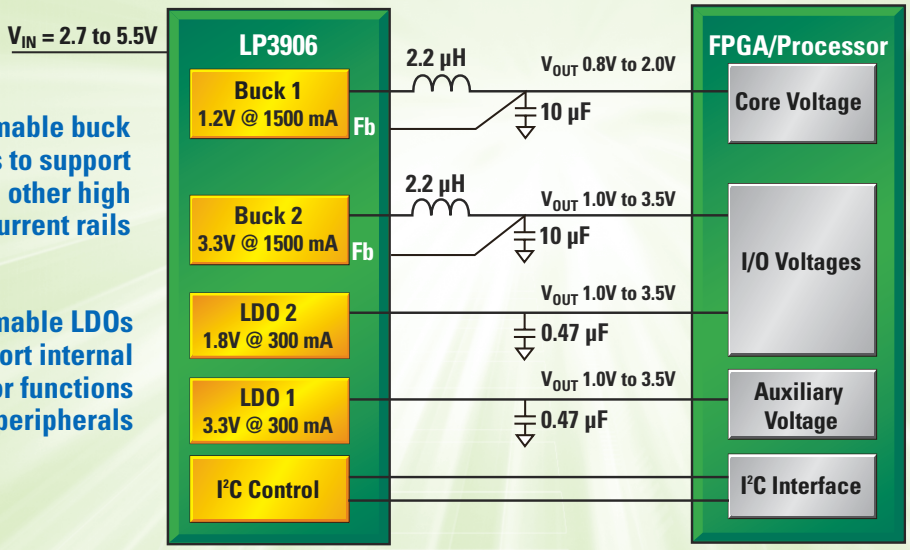

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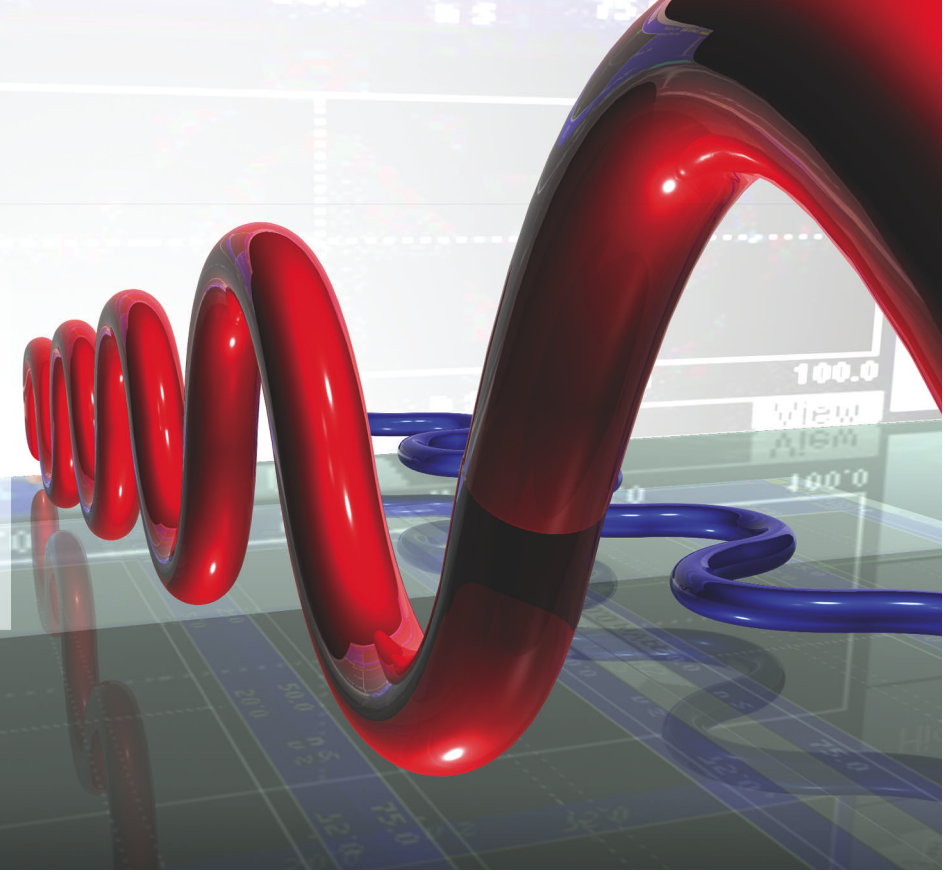

EDN VOICE OF THE ENGINEER 50 years

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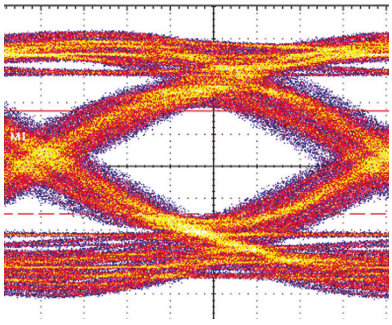
9.14.06



Abracadabra: making system interconnect disappear with FPGAs

by Andy Turudic, Altera Corp

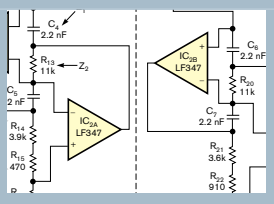
Making waves: Eight years later, details still matter

by Dan Strassberg, Contributing Technical Editor

SDR goes to war

by Nicholas Cravotta, Contributing Technical Editor

DESIGNIDEAS



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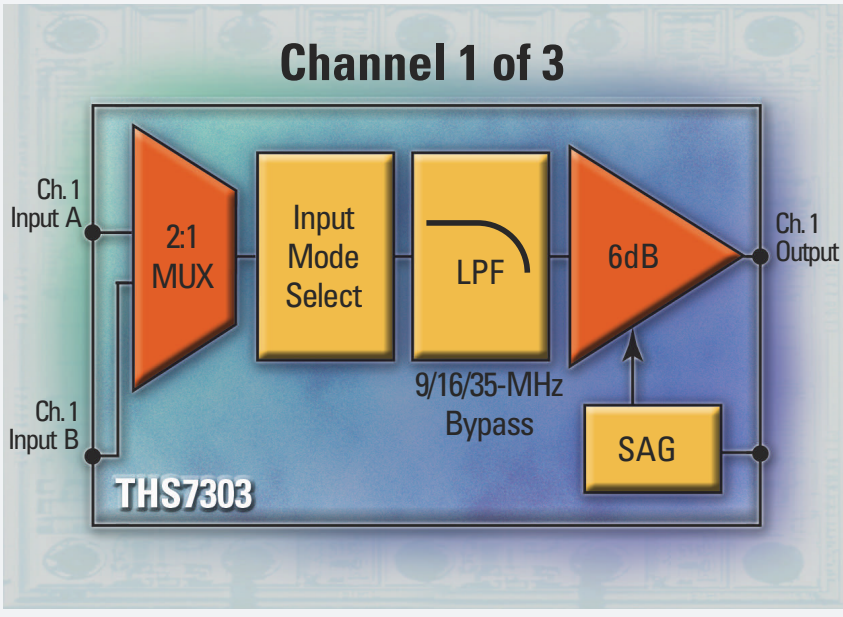

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Device	# of Channels	Filter -3 dB Freq (MHz) (typ)	# of Filter Poles	Bypass Bandwidth (MHz) (typ)	Gain (dB)	Input Coupling	Output Coupling	SAG Output	Price Starts at 1K
THS7303	3	9, 16, 35	5	190	6	AC-Bias, AC-STC, DC, DC+Shift	AC or DC	Yes	$1.65
THS7313	3	8	5	–	6	AC-Bias, AC-STC, DC, DC+Shift	AC or DC	Yes	$1.20
THS7353	3	9, 16, 35	5	150	0, Adjustable	AC-Bias, AC-STC, DC, DC+Shift	AC or DC	No	$1.65

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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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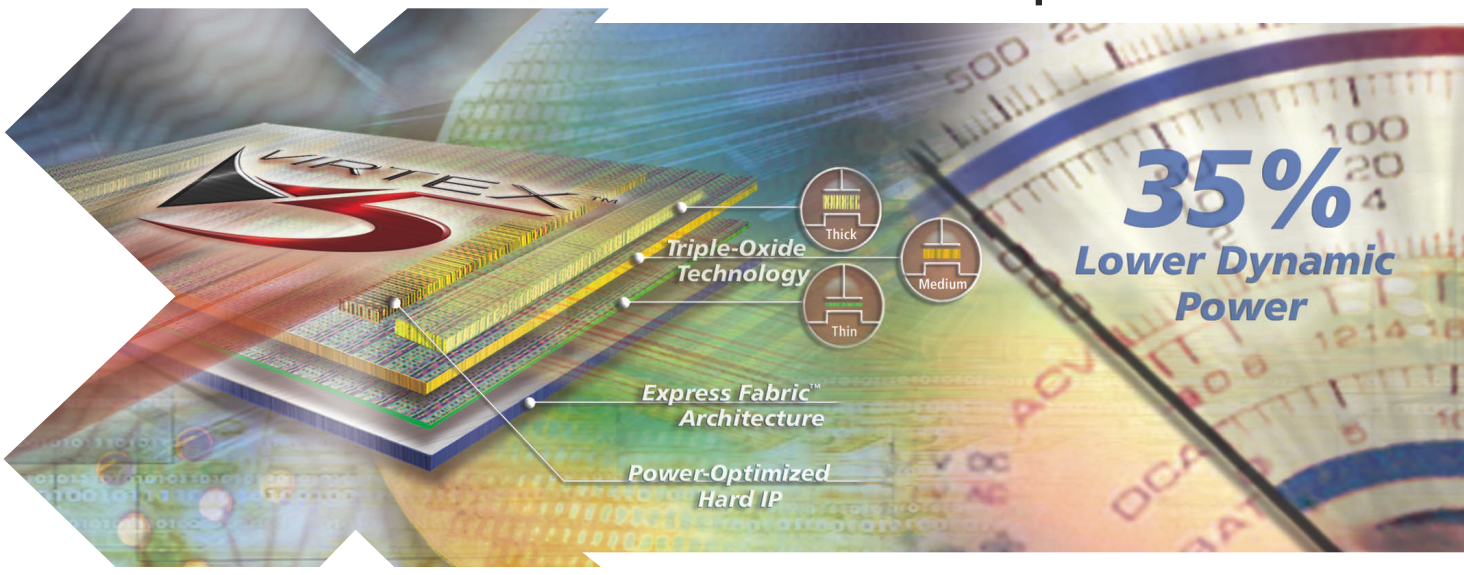

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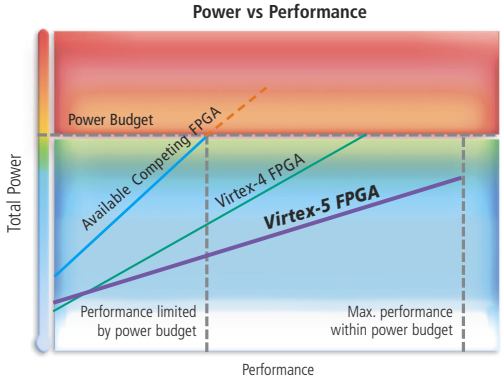

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Vol. IV, Issue 9

DESIGN idea

Optimizing Portable Applications with D/A Converters

By Chuck Sins, Applications Engineer

Designers of portable electronic devices have several methods available for using general-purpose Digital-to-Analog Converters (DACs) to digitally adjust voltages and enhance the performance of portable devices.

DACs are most easily understood by examining a simplified DAC block diagram. As shown in ***Figure 1***, the architecture of a one-channel DAC consists of a resistor array (each of equal value R) followed by a rail-to-rail voltage output amplifier. The voltage applied to the reference pin is the voltage at the top of the resistor array and a switch is connected between each pair of resistors and one to ground. The voltage is tapped off by closing one of the switches and connecting this point on the array to the amplifier. The resistor array and output amplifier consume very little power and emit no switching noise since the DAC is static once the specified resistor tap has been connected to the amplifier. In addition, multi-channel DACs packaged in a 3 mm by 3 mm Leadless Leadframe Package (LLP®) occupy very little board space in portable applications. An alternative to using a DAC is a resistive trim potentiometer. However, these devices are large in size, suffer from mechanical wear, and are not digitally controllable.

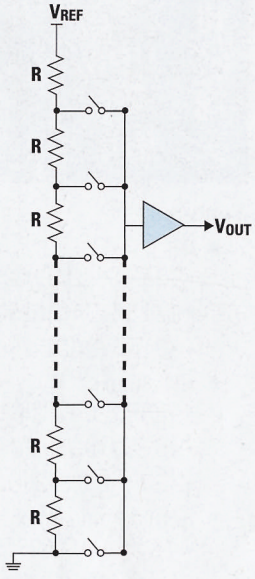

Figure 1. 1-Channel DAC Architecture

Over the last couple of years, the audio capability and LCD display quality of cell phones have improved tremendously, while the size and cost of the phones have gone down. Most phones today have a headphone jack, an earpiece, and a built in loudspeaker. All three of these audio outputs require some type of volume control. One way a DAC can provide volume control is when it is used in conjunction with an audio amplifier that has a built-in DC volume control. A micro-controller that receives input from soft keys on the display or push buttons on the case causes the DAC's output voltage to step up or down (***Figure 2***). Another way to control volume is to use a DAC as a single quadrant multiplier. This configuration consists of an amplifier gain stage that feeds the amplified audio input into the reference pin of the DAC (***Figure 3***). The Serial Peripheral Interface (SPI) of the DAC is used to digitally attenuate the amplified audio input anywhere from full scale (0 dB) to zero volts. This is accomplished without adding any noticeable level of noise or distortion to the audio signal.

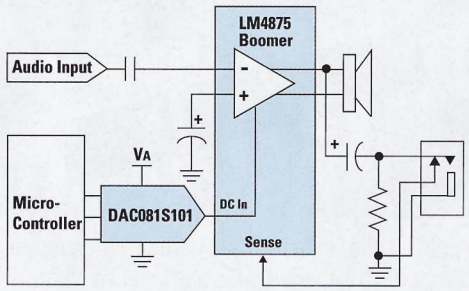

Figure 2. DC-Control of an Audio Amplifier

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Closed-Loop Bandwidth Accuracy

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Featured Products

1-Channel, Pin- and Function-Compatible DACs Across Resolutions

The 1-channel, pin- and function-compatible 8-, 10-, and 12-bit DACs each provide rail-to-rail output swing and input clock rates of 30 MHz over the entire supply range of 2.7V to 5.25V. The reference for each is derived from the power supply, resulting in the widest possible dynamic output range. A power-down feature reduces power consumption to less than 0.2 µW, which is especially important for portable, battery-powered applications.

The on-chip output amplifier allows rail-to-rail output swing and the three-wire serial interface operates at clock rates up to 30 MHz over the specified supply voltage range and is compatible with standard SPI™, QSPI, MICROWIRE, and DSP interfaces. The supply voltage serves as its voltage reference, providing the widest possible output dynamic range.

Features

- Settling time: 10 µs
- Guaranteed monotonicity
- Low-power operation
- Rail-to-rail voltage output
- Power-on reset to zero volts output
- SYNC interrupt facility
- Wide power supply range: 2.7V to 5.5V
- Power down feature

Operating over the extended industrial temperature range of -40°C to +105°C, these DACs are ideal for battery-power instruments, digital gain and offset adjustment, programmable voltage and current sources, and programmable attenuators. The DAC121S101, DAC101S101, and DAC081S101 are available in TSOT-6 and MSOP-8 packaging.

For FREE samples, datasheets, and more, visit
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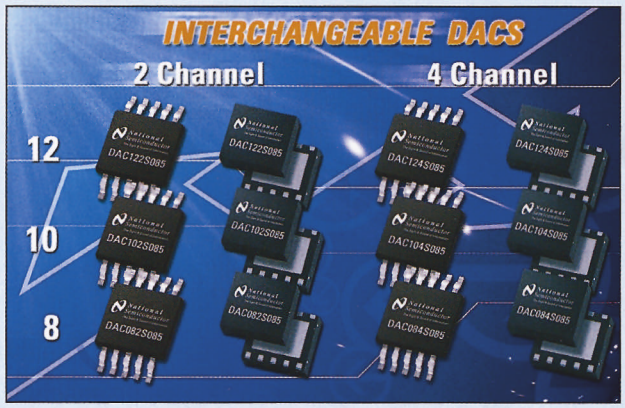
www.national.com/pf/DC/DAC101S101.html
www.national.com/pf/DC/DAC081S101.html

Ultra Low-Power, 2-Channel, 8-/10-/12-Bit DACs

These general purpose DACs are full-featured and can operate from a single 2.7V to 5.5V supply and use 210 µA at 3V and 320 µA at 5V. The on-chip output amplifier allows rail-to-rail output swing and the three-wire serial interface operates at clock rates up to 40 MHz over the entire supply voltage range.



Features

- INL (max)
  - ±0.5 LSB (DAC082S085)
  - ±2 LSB (DAC102S085)
  - ±8 LSB (DAC122S085)
- DNL (max)
  - +0.18 / -0.13 LSB (DAC082S085)
  - +0.35 / -0.25 LSB (DAC102S085)
  - +0.7 / -0.5 LSB (DAC122S085)
- Settling time (max)
  - 4.5 µs (DAC082S085)
  - 6 µs (DAC102S085)
  - 8.5 µs (DAC122S085)
- Zero code error: +15 mV (max)
- Full-scale error: -0/75% FS (max)
- Wide power supply range: 2.7V to 5.5V

The 2-channel, 8-/10-/12-bit DACs are ideal for use in battery-powered instruments, digital gain and offset adjustments, programmable voltage and current sources, and programmable attenuators. The DAC082S085, DAC102S085, and DAC122S085 are available in MSOP-10 and LLP-10 packaging.

For FREE samples, datasheets, and more, visit
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Optimizing Portable Applications with DACs

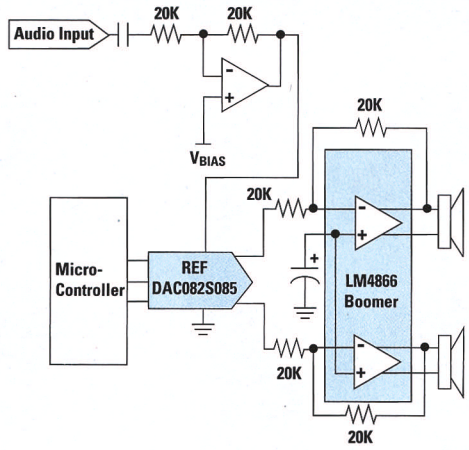

Figure 3. Single Quadrant Multiplying DAC

Many microprocessors can operate at a lower supply voltage to save power, and then operate at a higher supply voltage to increase their processing speed. Switching between these modes requires adjusting the output voltage of a DC-to-DC converter. Similar to microprocessors, LCD displays utilize DACs to control their contrast ratio. As the temperature of the display changes, the voltage applied to the display by the DC-to-DC converter must be adjusted to maintain the proper contrast ratio (*Figure 4*). Since neither of these applications require high speed adjustments, general purpose DACs are the ideal solution for digitally optimizing their performance.

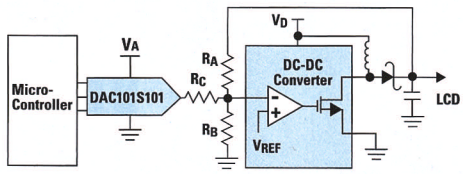

Figure 4. DAC Controlling a DC-DC Converter

Portable devices that utilize sensors can also be enhanced with the use of general purpose DACs. *Figure 5* illustrates a pressure sensor that is amplified and then monitored by a general purpose Analog-to-Digital Converter (ADC). Since the output of the amplifier stage has a large voltage range, the ADC requires a reference voltage equal or greater to the largest possible output voltage. While this is fine for measuring the sensor's output when it is at its maximum voltage, it is less than ideal for measuring the sensor's minimum output voltage. If a DAC was utilized as the reference voltage, the DAC could be digitally adjusted based on the input to the ADC. This technique maximizes the accuracy of the ADC and allows the full range of codes to be utilized. The alternative solution is to use a more expensive ADC with a higher resolution in order to improve the system's accuracy. As a result, using a DAC in the circuit reduces the overall system cost while still providing the required accuracy.

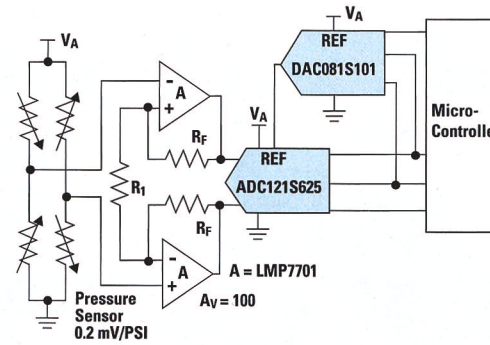

Figure 5. Pressure Sensor Monitoring by an ADC

A similar application with a DAC enhancing system performance is a system that requires calibration for higher conversion accuracy. For example, a humidity sensor can be calibrated to a known ADC output code with the circuit in *Figure 6*. The sensor's output is applied to the negative input of the op-amp while a DAC output is connected to the positive terminal. The desired output code of the ADC can be achieved by digitally adjusting the DAC output voltage to the appropriate level. Higher resolution DACs deliver higher precision in the output reading.

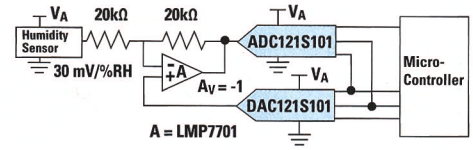

Figure 6. Humidity Sensor Application

In all of these examples, general purpose DACs optimized a product's performance by digitally adjusting a voltage in the circuit without impacting the product's size, cost, or power consumption. ■

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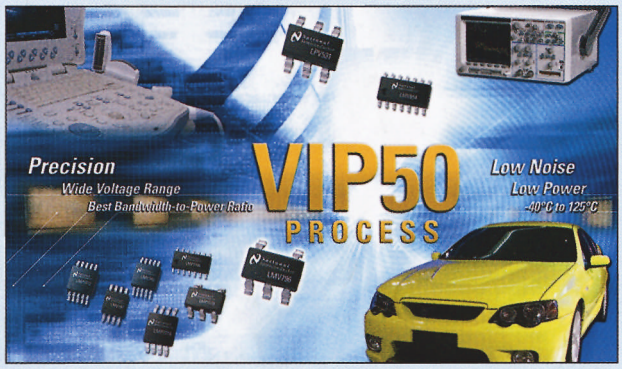
The LMP7701/02/04 are single, dual, and quad low offset voltage, rail-to-rail input and output precision amplifiers with CMOS input stage and wide supply voltage range. The rail-to-rail input stage significantly reduces the CMRR glitch commonly associated with rail-to-rail input amplifiers.



Features

- Input offset voltage (max)
  - ±200 µV (LMP7701)
  - ±220 µV (LMP7702/04)
- Input bias current: ±200 fA
- Input voltage noise: 9 nV/$\sqrt{\text{Hz}}$
- 130 dB CMRR
- 130 dB open loop gain
- 2.5 MHz unity gain bandwidth
- Supply current
  - 715 µA (LMP7701)
  - 1.5 mA (LMP7702)
  - 2.9 mA (LMP7704)
- Supply voltage range: 2.7V to 12V

The LMP7701/02/04 are ideal for high impedance sensor interfaces, battery-powered instrumentation, high gain amplifiers, DAC buffers, instrumentation amplifiers, and active filters. The LMP7701 is available in SOT23-5 packaging, the LMP7702 is available in MSOP-8 packaging, and the LMP7704 is available in TSSOP-14 packaging.

For FREE samples, datasheets, and more, visit
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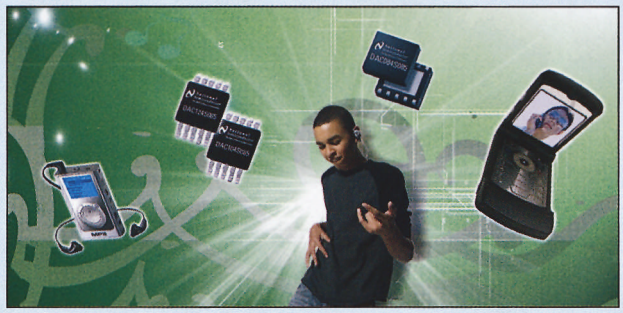

Ultra Low-Power, 4-Channel, 8-/10-/12-Bit DACs

These 4-channel, 8-/10-/12-bit DACs are full-featured and can operate from a single 2.7V to 5.5V supply and use 360 µA at 3V and 480 µA at 5V. The on-chip output amplifier allows rail-to-rail output swing and the three-wire serial interface operates at clock rates up to 40 MHz over the entire supply voltage range.

The reference serves all four channels and can vary in voltage between 1V and VA, providing the widest possible output dynamic range. A power-down feature reduces power consumption to less than a microWatt with three different termination options.

Features

- INL (max)
  - ±0.5 LSB (DAC084S085)
  - ±2 LSB (DAC104S085)
  - ±8 LSB (DAC124S085)
- DNL (max)
  - +0.18 / -0.13 LSB (DAC084S085)
  - +0.35 / -0.25 LSB (DAC104S085)
  - +0.7 / -0.5 LSB (DAC124S085)
- Settling time (max)
  - 3 µs (DAC084S085)
  - 4.5 µs (DAC104S085)
  - 6 µs (DAC124S085)
- Zero code error: +15 mV (max)
- Full-scale error: -0/75% FS (max)
- Wide power supply range: 2.7V to 5.5V

The 4-channel, 8-/10-/12-bit DACs are ideal for use in battery-powered instruments, digital gain and offset adjustments, programmable voltage and current sources, and programmable attenuators. These DACs are available in MSOP-10 and LLP-10 packaging.

For FREE samples, datasheets, and more, visit
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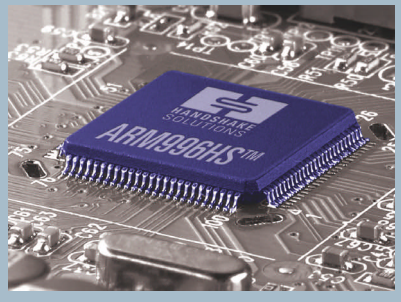

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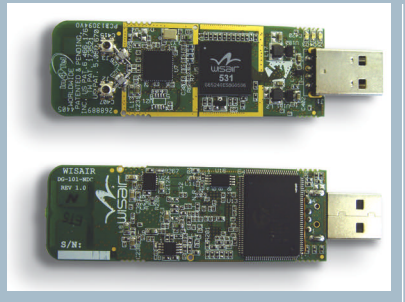

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BY MAURY WRIGHT, EDITOR IN CHIEF

Kamen clobbers big-company management

As I promised in a previous column, I'll share some of Dean Kamen's thoughts on innovation, management, and leadership (**Reference 1**). Kamen is the founder of DEKA (Dean Kamen) Research and Development Corp (www.dekaresearch.com) and the inventor of the two-wheeled Segway human-transportation device. Kamen delivered an entertaining and enlightening keynote at last month's National Instruments Week conference in Austin, TX.

Early in his talk, Kamen discussed the typical project and inevitable dark times when success seems out of the question. He playfully suggested that when you plan a project that you "schedule a miracle." His message was about believing in and sticking with your idea. He quoted Winston Churchill, who said, "When you are going through hell, keep going."

Kamen presented a mythical project that a team plans over five years. After six months, the team is 10% into the project. "You'll never have an opportunity to know as much incremental new stuff as you did in the first six months because the denominator was zero," said Kamen. He contends that the 10% point is the best time to change the schedule or project. During those six months, the team may have figured out that the tasks are easier than expected or that bigger obstacles stand in the way. "At the end of six months, changing to four years or six years wouldn't be a big deal," he stated. He claimed that the impact is minor because the team is small; the burn rate is low; and the project hasn't incurred expenses for tooling, marketing, and other cost centers. He quipped, "I've never seen anybody do that. I've still got four years left to fix it; besides, it won't be my problem by then."

Kamen pointed out that a team more typically gets four and a half years into the project, when it's painfully clear that the project can't launch on time, and then changes the schedule. "It's the most expensive—the most painful time to do it," he said. The story drew laughs and applause from the crowd, who Kamen immediately challenged, asking, "You mean to tell me that any project that you've ever seen that finally was launched late, that you blew the whistle and made the changes as early as possible with the least risk cost? I don't think so—never works that way."

Although Kamen was advising better decision-making, he also suggested another way to prevent schedule slippage. He suggested: "Invent as a last resort." These days, especially with the Internet, someone else may have solved the individual problems that you face. Kamen also cautioned that you approach projects without preconceived bias. He related the story of a dialysis machine that DEKA redesigned. The earlier design used tubes that allowed fluid to flow "even when tied in a knot," and it also relied on compressing the tubes so that they worked as valves. Kamen related that the customer thought it wanted DEKA to solve its problem, but, in reality, the customer wanted him to fix its solution. DEKA ultimately delivered a different design. "It's not what we don't know that inhibits innovation; it's what we do know that just ain't so," he said.

Regarding management and leadership and their effect on innovation, Kamen stated, "Projects in big companies do require management. But innovation requires leadership, and I think they're not only not the same, they are diametrically opposed. ... Management is a process by which we make sure everything comes out the same. ... Good management would be to give a machine gun to an ax murderer; it would make the process more efficient. ... Management is doing things right. Leadership is doing the right things. Innovation, which is hard to do, is particularly hard to lead."

Kamen encourages innovation despite the inherent difficulty, pointing out that innovation creates entire industries. But he also asked: When should you innovate? The answer is now. He pointed out that, in his 30 years of experience, no one has ever asked him to work on the next-generation product while the current product is selling well and cash flow is great. Instead, he hears, "We're going to be toast in six months unless we do something. We've got to have a radically new idea. It's got to be out there, we don't have a lot of time, we don't have a lot of money, and you better get it right."

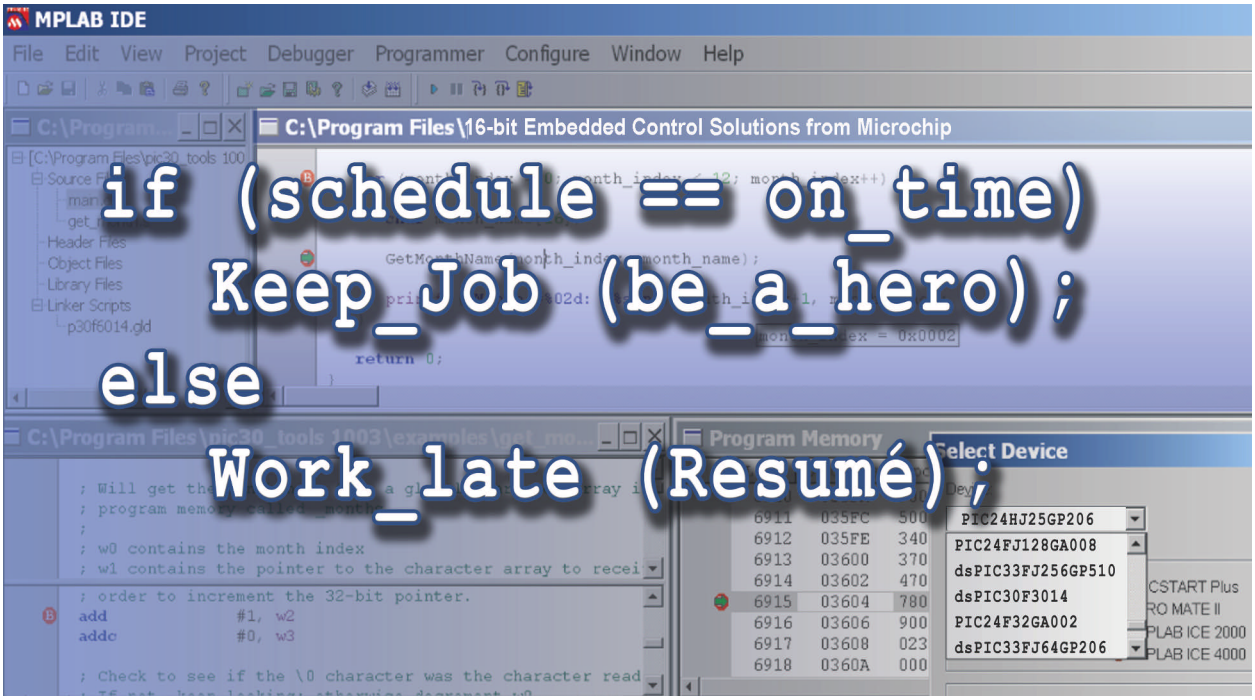
Finally, Kamen champions risk takers. "You don't define success as the lack of failure," he said. Unfortunately, management is about not trying to fail. He pointed out that optimists such as the Wright brothers were willing to fail—without killing themselves—and the aviation industry was born. EDN

REFERENCE

1 Wright, Maury, "Sportslike competition drives science and technology education," *EDN*, Sept 1, 2006, pg 12, www.edn.com/article/CA6363908.

You can reach me at 1-858-748-6785 or mgwright@edn.com.

Stay on Schedule



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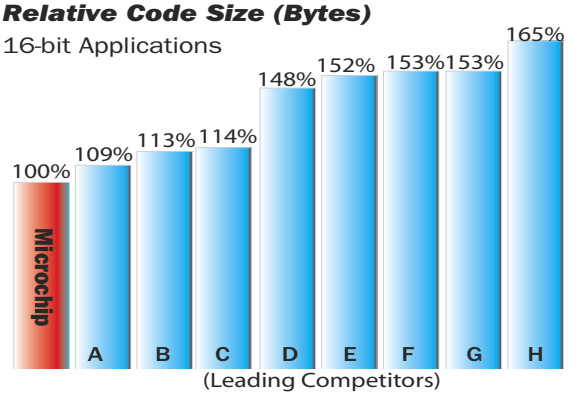

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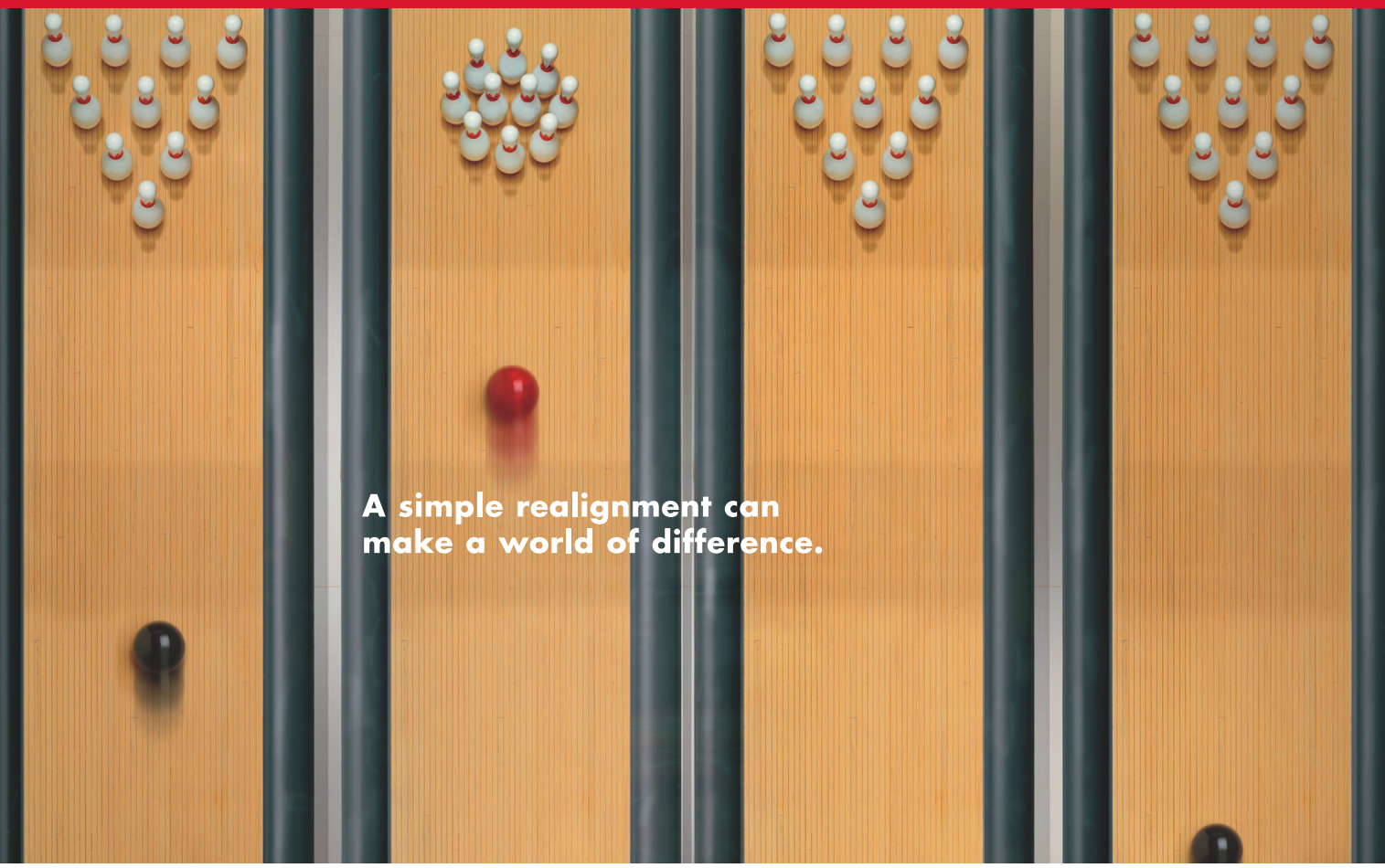
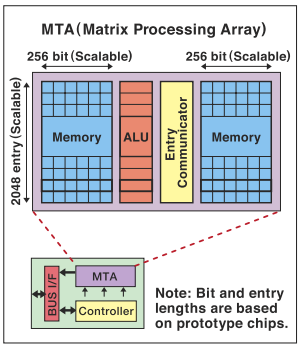


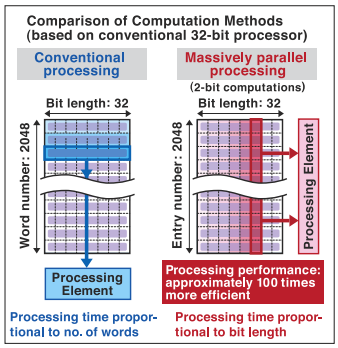
Taking a new approach to matrix architecture by placing an ALU between memory components, Renesas Technology redefines graphics processing potential.

Multimedia data processing is the magic that makes consumer products such as digital movie cameras so exciting. It involves high-level arithmetic operations, including fast-Fourier transforms and convolution. Ordinarily, these essential calculations are handled by a specialized digital signal processor (DSP). But ever-increasing pixel counts and a proliferation of multimedia data standards have pushed the humble DSP to its limits. It's time to advance to a new processing paradigm.

Leading that advance is Renesas Technology, with a massively parallel processor based on a matrix architecture that combines the processing performance of hardwired logic with DSP-like programmability. The unique design of this processor places an arithmetic logic unit (ALU) between memory components to handle arithmetic operations and enable simultaneous spatial processing of data aligned in parallel.



Massively parallel processing: Matrix architecture
Revolutionary placement of an ALU between memory components eradicates data transfer bottlenecks.



Massively parallel processing: Bit-serial, parallel-entry
Achieving simultaneous spatial processing, as opposed to processing of data from top to bottom.

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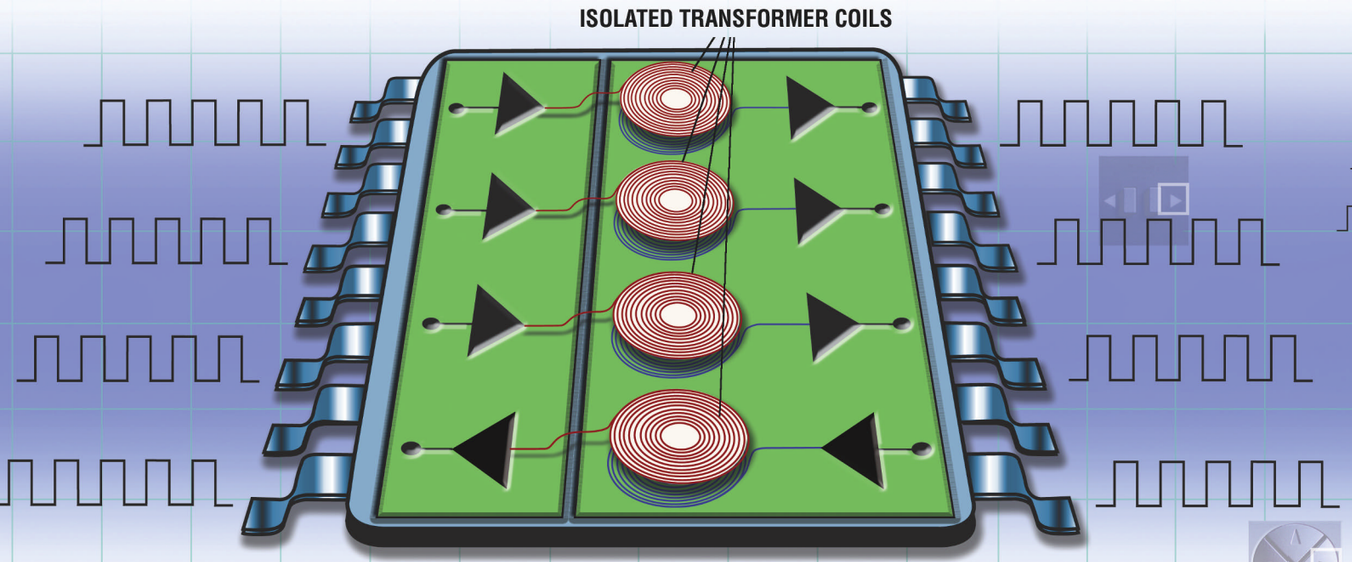

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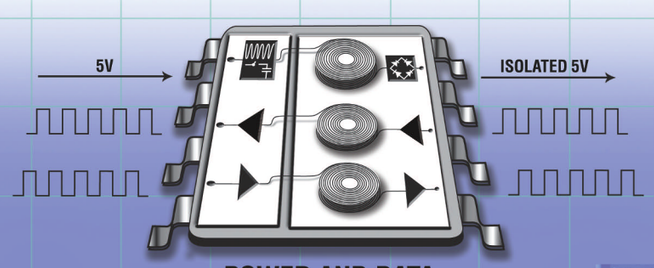
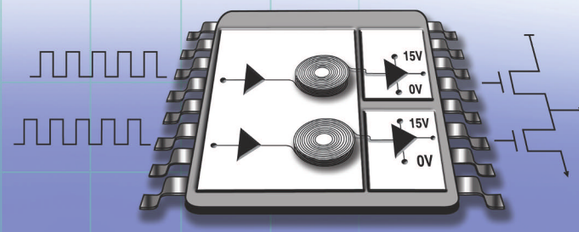
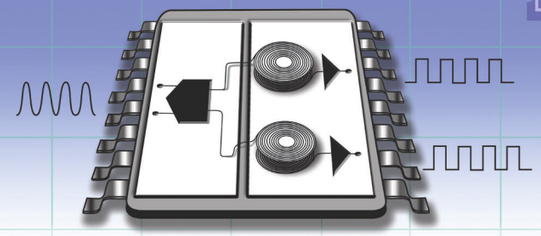


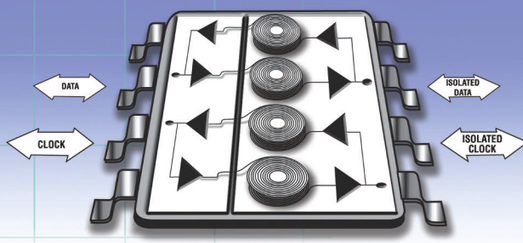
POWER AND DATA



GATE DRIVERS



CONVERTERS



COMMUNICATIONS

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Never stop thinking

Test set speeds next-generation wireless-device calibration

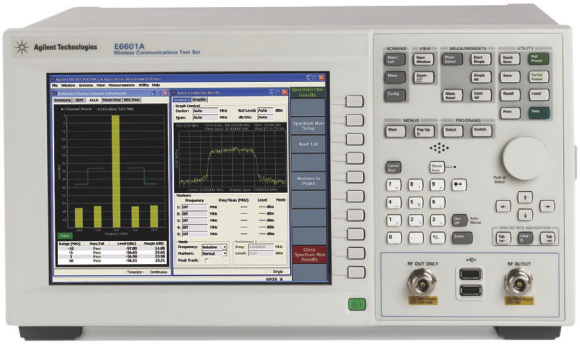
Agilent Technologies has announced the availability of a next-generation wireless-communications test-set platform, which the company calls ideal for calibrating mobile phones in high-volume manufacturing. The test set provides industry-leading measurement speed and integrity as well as unique scalability—all targeting a decrease in the manufacturing cost of test.

The Agilent E6601A is an integrated test system in one box. It features a built-in, open-Windows XP PC, which allows the development, downloading, and execution of test programs directly in the system—eliminating the test-system PC and saving system space and cost. With a new measurement architecture that Agilent says targets high-speed measurements and accuracy, repeatability, and measurement integrity, the unit significantly lowers the cost of mobile-phone manufacturing test. In addition, the product provides reliability and low cost of ownership, the company claims.

One of the test set's key features is its speed—as much as 30% faster than other approaches. New calibration applications for GSM (Global System for Mobile communications), GPRS (General Packet Radio System), EGPRS (Enhanced GPRS), WCDMA (wideband code-division multiple access), and HSDPA (high-speed data-packet access) provide scalable, multiformat capabilities with only a software upgrade. For mobile-phone calibration, an optional fast device-tune measurement enables speeds as great as 10 times those of traditional methods. Connectivity is possible through 100BaseT LAN, IEEE 488, and six USB 2.0 ports.

The E6601A is the newest addition to Agilent's wireless-communications test-set product line, which includes the 8960 wireless-communications test set. As the company's flagship product, the 8960 continues to suit applications for wireless-device R&D, conformance test, manufacturing, service, and support. The E6601A costs $27,100. A GSM/GPRS-calibration application costs $6000, and a WCDMA-calibration application costs $6000.**—by Dan Strassberg**

▷**Agilent Technologies**, www.agilent.com.



The E6601A is a one-box integrated test system for next-generation mobile-communications devices.

Dual computers boost system performance

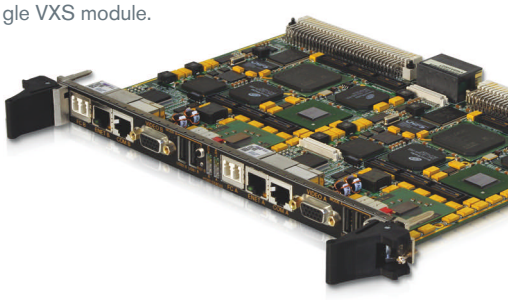
Many aerospace and military applications require redundant or parallel processors to achieve extended availability requirements and meet performance goals. So, why not include redundant hardware on a single board? General Micro Systems has accomplished that task with the new V469 Patriot VXS (VME-switched-serial) dual-processor, single-board computer. The company claims that the board provides the highest "horsepower density" per watt of any other current technology.

Unlike other dual-processor boards, Patriot uses two independent M-760 Pentium M processors that offer 100% redundancy, including power, cooling, and I/O. Each half operates at 2 GHz and has its own Fibre Channel connection with boot capability. The two halves communicate through a direct gigabit-Ethernet link. Support for the Patriot is available under Windows XP/2000, VxWorks-Tornado II, and Linux. Prices start at $4700 (100).

—by Warren Webb

▷**General Micro Systems Inc**, www.gms4sbc.com.

The V469 Patriot single-board computer packs two independent Pentium M processors plus peripherals onto a single VXS module.



Hall-effect hot-swap controller debuts

The new ACS760 series of ICs from Allegro Microsystems incorporates Hall-effect sensing to control inrush and protect the power buses in blade servers and other applications. This IC provides a major advantage over other approaches, which use a dropping resistor to yield a current measurement. These resistors are expensive, take up board space, and generate heat. Using a copper-board trace as the resistor is futile because the large TCR (temperature coefficient of resistance) of copper and the variation in board production make this method inaccurate and unreliable. In addition, engineers must design copper traces leading to the resistors to remove the resistor's heat. This approach takes up even more board space and creates a hot area that customers may perceive as a design shortcoming.

When you use these resistors in blade servers and other high-density systems, all the heat from the sensing resistors can increase the budget for cooling fans and other peripherals. Heat also shortens semiconductor lifetimes in direct proportion to the heat at which they operate.

In addition, any dropping-resistor scheme must galvanically connect to the bus, unless you design in complex and expensive isolation circuits. Optoelectronics all age significantly over their lifetime, making a stable, accurate, long-term isolation scheme a challenge to design. Allegro's ICs sense the magnetic field that the current flowing in the conductor creates and isolate the chip's power and output from the high-current bus. This approach can allow isolation to the bus if a user designs in the simpler isolation scheme for the bus NFET.

The ACS760ELF-20B can provide 240 VA of protection and inserts only 1.5 mΩ of resistance into the bus. In addition to controlling the gate of the N-channel high-side bus FET, it provides an analog-voltage output proportional to the signal. It also contains an overcurrent comparator that you can use to provide a digital trip point. An internal charge pump provides above-the-rail voltage to control an N-channel high-side FET. The IC operates at 10.8 to 13.2V. The analog-signal bandwidth is 50 MHz, and the circuit, including 12 pins for the dc bus, fits into a thin, 24-pin QSOP.

The first part in a future family, the ACS760 targets low-voltage bus control, so it does not take advantage of the isolation that Hall sensing provides. Instead, it differentially senses the voltage at the load, so that it can account for the power calculations to provide thorough bus control. Allegro expects the ACS760ELF-20B to sell for $2.48 (10,000).

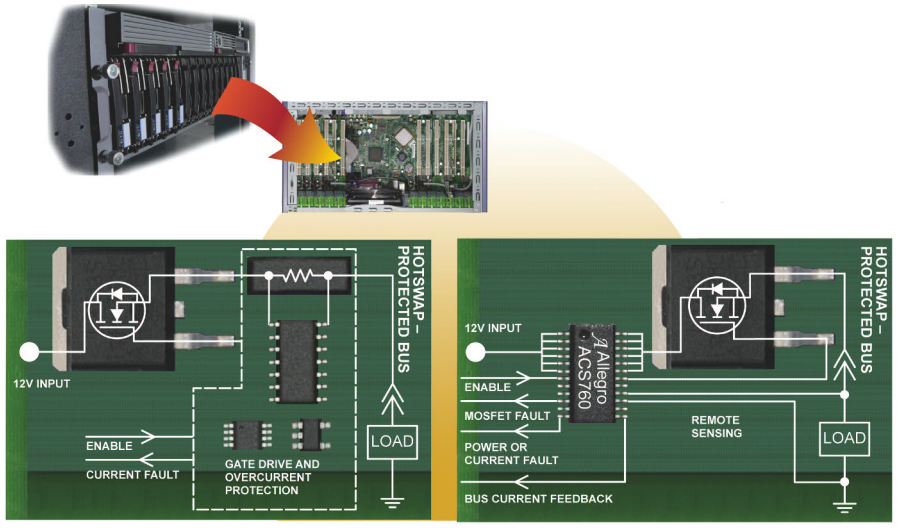
—by Paul Rako

▷**Allegro Microsystems**, www.allegromicro.com.

FROM THE VAULT

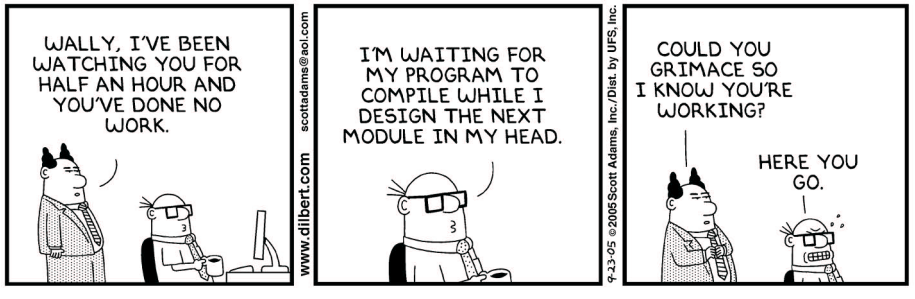
DSP ICs have reached the same point in their evolution that the μP had attained in the early 1970s, when the 8008 had demonstrated the promise of 8-bit general-purpose μPs but the 8080 had yet to appear. The recent appearance of a DSP chip from Texas Instruments could mark the start of general-purpose use of DSP devices.

Robert Cushman, Special Features Editor, *EDN*, July 16, 1982, pg 44



In contrast to a traditional approach using dropping resistors (left), the ACS760 IC (right) uses Hall-effect-sensing resistors to sense the current and control the bus power in hot-swap applications.

DILBERT *By Scott Adams*



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32-nm CMOS begins to take shape

At the Semicon West conference in San Francisco in July, the dim outlines of 32-nm CMOS began to take shape. The process will look more familiar to design teams than many had predicted, but the process is still far from business as usual. Pacing the still-tentative discussion of 32-nm technology, Applied Materials proclaimed that 32-nm processes would continue to use planar MOSFETs. This claim represents a major change from conventional wisdom, which declares that the 32-nm process signifies the dawn of the 3-D, multigate transistor. FinFETs, trigate MOSFETs, and fully depleted SOI (silicon-on-insulator) devices were all aiming to hit the mainstream at this process node.

All of these devices increase the gate's control over channel current. As channels got shorter and gate dielectrics got thinner, device physicists tried making the channel as thin as possible and surrounding it with gate electrodes to help the electric field from the gate to pinch off the channel current. The vendors thought that, with the advent of the 32-nm-process node, this approach would keep the ratio of saturation current to leakage current high enough for the transistors to be useful.

You can track the change in plans to two factors. First, the multigate devices have proved more problematic than early research suggested. The 3-D structures are difficult to fabricate reliably in the presence of production-process variations. But another problem has emerged, according to Ludo Deferm, vice president of business development at European consortium IMEC (Interuniversity Microelectronics Centre). Deferm observes that the structure of the multigate devices and fully depleted SOI transistors effectively isolate their channel regions from the underlying bulk silicon. This characteristic makes it difficult or impossible to drive contaminant atoms from the channels into underlying bulk material. The channels are so thin that the inability to purge defective atoms seriously reduces yield expectations for large dice.

Meanwhile, another factor—progress in using strain engineering to improve the saturation current of planar devices—appears to be shoving multigate devices beyond the 32-nm-process horizon. At Semicon, both IMEC and Applied Materials reported work to increase the stress on channels in planar transistors to more than 1G pascal, doubling the channel-carrier mobility in one example.

This work yields two surprising advances. First, it shows that applying two techniques—stress-reducing caps over recessed sources and drains, and over-the-top etch-stop layers—to one transistor can result in more than additive increases in mobility. Second, the work at Applied Materials demonstrates improvements for both N- and P-channel devices. The company uses silicon-carbon epitaxial caps over the recessed source and drain and a tensile nitride-etch-stop layer over the top of the NMOS device, resulting in a tensile stress of 1.2G pascal. The company uses a similar structure, but with silicon-germanium epitaxy and a compressive-nitride layer, on the PMOS device. In both cases, the applied stresses are biaxial. The results are 32-nm planar P- and N-channel transistors with adequate mobility to build circuits.

However, it won't be easy for the process engineers or the circuit designers. Faran Nouri, director of Applied Materials' Applications Development Center, says that, although the company has separately fabricated N- and P-channel devices and measured their saturation currents, it has not yet fabricated them on the same wafer. Some process-integration issues will occur, she says, but the company expects no "showstoppers." Using the resulting transistors will be an issue, as well. One primary concern is the constraints that the devices will put on layout, at both the cell and the chip levels. The effect of stress on mobility depends on the orientation of the stress vector in the crystal lattice. So, the mobility of a transistor can depend on its orientation on the wafer.

More seriously, the actual stress on the channel—which the company can only simulate, not measure directly at these dimensions—highly depends on the geometry of the epitaxial caps, the etch-stop layer, and even the surrounding structures. This dependence makes the performance of each transistor on a die dependent on the geometry that surrounds it. Applied is now working with Synopsys (www.synopsys.com), and it's a good bet that other developers are also scrambling to try to figure out how to shield cell-layout engineers and circuit designers from this issue. The result could be vastly more complex placement-and-routing algorithms, the need for draconian placement and orientation rules, or both.

In addition, the enhancements to mobility of both N- and P-channel devices are changing the beta ratio, which depends on the ratio of N- to P-channel mobility. But that ratio underlies the basic design of CMOS circuits. Nouri says that the ratio is changing in today's processes, and it will continue to change. By the 32-nm node, it will have changed enough to demand new circuit topologies for many common digital structures and will have uprooted current analog topologies. The future may be bleak, but it is probably happier than that for multigate transistors with their own circuit characteristics and profound issues.

—by Ron Wilson

▷**Applied Materials**, www.amat.com.

▷**IMEC**, www.imec.be.

FROM THE VAULT

"You can create efficient single-chip implementations of complex circuits. ... Semicustom-IC technology might represent the high-tech equivalent of Ben Franklin's proverbial Philosopher's Stone. ... You can now easily create fast-turnaround, inexpensive, and well-characterized customized ICs without directly designing detailed geometric masks."

Andy Rappaport, *EDN*, Feb 17, 1983, pg 79

The FPGA Eye Opener!

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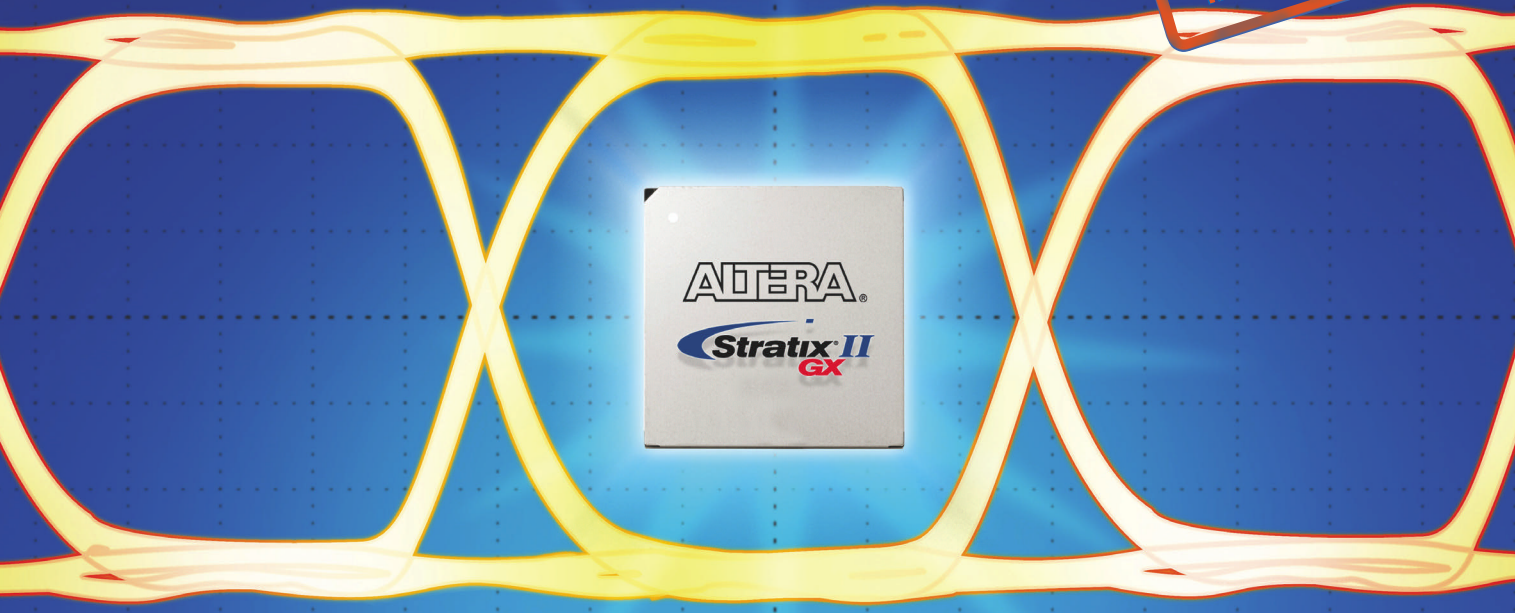

Transmit eye diagram at 6.375 Gbps. For characterization details, see www.altera.com/stratix2gx/characterization.

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RESEARCH UPDATE

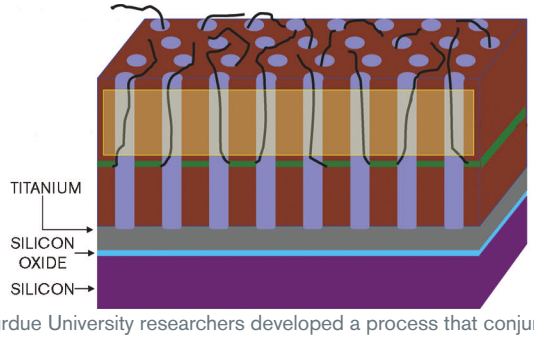
BY MATTHEW MILLER

Process coaxes carbon nanotubes into service as vias

Researchers at Purdue University have developed a process that grows individual carbon nanotubes vertically atop a silicon wafer. Step 1 in the process uses anodization to create an array of cylindrical pores in a thin film that features a small layer of iron between two layers of aluminum. In Step 2, the researchers flow a mixture of hydrogen and methane into the pores and use microwave radiation to break down the methane. The iron layer then acts as the catalyst for a reaction that causes carbon from the methane to self-assemble into carbon nanotubes.

The resulting vertically oriented nanotubes become, in essence, vias that could connect stacked electronic components. As with most other research involving carbon nanotubes, however, big unknowns remain. The Purdue researchers acknowledge, for example, that scientists have yet to figure out how to integrate carbon nanotubes with other types of circuitry and devices.

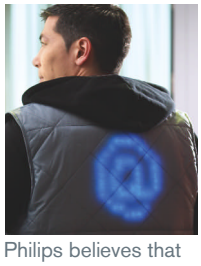
▷**Purdue University**, www.purdue.edu.



Purdue University researchers developed a process that conjures carbon nanotubes that could serve as interconnects for vertically oriented circuits.

Your name in lights, on your body

Philips Research has demonstrated jackets featuring its Lumalive textiles, which integrate flexible arrays of LEDs into the fabric. The jackets feature 200×200-mm color panels and discreetly concealed battery and electronics packs that the user can, we hope, remember to disconnect and remove before washing.



Philips believes that its LED-animated textiles are where it's @.

The company states that the production-ready technology can scale to illuminate drapes, cushions, or even an entire sofa "to enhance the observer's mood and positively influence his behavior." We wonder how long it will be before an entrepreneurial hacker couples one of the jackets with a wireless connection and becomes a walking billboard.

▷**Philips Research**, www.research.philips.com.

Magnetic material may put new spin on computing

Researchers at the Massachusetts Institute of Technology have developed a magnetic semiconductor that could bring electron "spin," which engineers already exploit in storage applications, into the realm of information processing.

The material—indium oxide with a dash of chromium—is compatible with silicon and can inject electrons of a given spin into silicon at room temperature, according to the researchers. Scientists expect that "spintronic" circuits, by encoding spin orientation in addition to current state, will deliver more computing power and versatility than traditional circuits. At the same time, because spin states are nonvolatile, spintronic circuits could drastically reduce power consumption.

The MIT group says that, although the material itself is promising, the true value of its work is more fundamental: The researchers uncovered the heretofore-elusive mechanism that governs the material's behavior.

▷**Massachusetts Institute of Technology**, www.mit.edu.

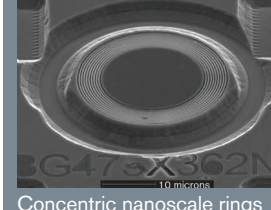
09.14.06

NANOSCALE CAVITY AMPLIFIES LED OUTPUT BY SEVEN TIMES

Precisely spaced grooves etched into a silicon cavity surrounding a semiconductor LED can make the LED as much as seven times brighter, according to researchers at NIST (National Institute of Standards and Technology).

Semiconductor LEDs typically emit only 2% of their light in the optimal direction, which is perpendicular to the diode's surface. So, NIST scientists fashioned a pattern of precisely carved and positioned grooves that causes reflections and interference that in turn shepherd more of the light in the right direction.

During several years of work honing the principle and the manufacturing technique, the scientists experimented with different arrangements of grooves. They eventually found that a structure including 10 grooves–each 240 nm wide, 150 nm deep, and 40 nm apart from each other–produces the brightest output. The invention could be especially helpful in medical-imaging applications in which brightness is crucial, according to NIST.



Concentric nanoscale rings surrounding a semiconductor LED can dramatically boost the LED's light output.

▶**National Institute of Standards and Technology,** www.nist.gov.

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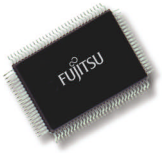

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Receivers target high-volume GPS and DVB-H applications

Chipidea, a silicon-IP (intellectual-property) provider in Lisbon, Portugal, has expanded its IP for RF-CMOS circuit blocks with two products for handheld designs. With its IP offerings in the logic space, this mixed-signal lineup achieves a new level of antenna-to-baseband capability, according to the company. Chipidea initially created both of its new designs for specific customers and has now "generalized" them into IP platforms for the wider market. Its mobile-TV platform has three receiver paths for 176 to 245 MHz, 470 to 870 MHz, and 1.450 to 1.685 GHz, supporting DVB-H (digital-video-broadcasting-handheld), DMB (digital-multimedia-broadcasting), and ISDB-T (Integrated Services Digital Broadcasting-Terrestrial) standards.

Chipidea's designers used a direct-conversion, zero-IF architecture that needs no external SAW or IF filter and have employed a fractional-N synthesizer that can use a crystal source from the host application as a reference, further reducing the external-component requirements. Operating from a 1.8 to 3.6V supply, the design uses approximately 60 mA.

The GPS (global-positioning-system)-receiver core will handle GPS and future Galileo signals in the L1 band. The receiver design's low-IF architecture needs no external IF filters. Because of the unit's low signal levels, you do need an external SAW filter, however. Power consumption is 20 mA; alternatively, if your design uses an active antenna that delivers an amplified signal, you can disable the built-in low-noise amplifier in the Chipidea IP to reduce that value to 15 mA. Chipidea is also developing an "all-systems-GPS" design that will accept ESA/ESB and E1/L1/L2, L2 and E1/L1/E2, or E6 and E1/L1/E2 signal groupings.

Chipidea initially fabricated both chips in TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) 0.18-micron CMOS, and it plans to follow the CMOS-process-migration path but only as is appropriate to the application. A DVB-H tuner is feasible in 90-nm technology, according to Vice President of Engineering Carlos Leme, but the low signal levels of GPS imply that 130 nm is the minimum geometry for that task, due to factors such as the process's noise figure.

—by Graham Prophet, *EDN Europe*

▷**Chipidea**, www.chipidea.com.

09.14.06

New US passports contain secure identification chips

Infineon Technologies has received a multimillion-piece purchase order from the United States government to supply technology for a new electronic passport. The new passports facilitate international travel by allowing automatic identity verification, faster immigration inspections, border protection, and security. The passports include a computer chip in the back cover that securely stores the same information that is printed on the document.

"The United States is helping to set the pace for adoption of more secure travel documents around the world," says Christopher Cook, managing director of Infineon Technologies North America. "As the leading supplier of the specialized chips used for secure personal identification, financial transactions, and access to electronic systems, our chips have successfully passed some of the most stringent security tests in the world. We are happy to be chosen to supply the electronics for the large-scale roll-out of the US electronic passport."

The electronic passport has multiple layers of security to protect the privacy of holders. These layers include basic-access control, which requires the border-control inspector to pass the document over a scanner that reads coded information and then authorizes the electronic reader to access the data stored on the chip. The actual data transmission occurs over a distance of about 4 in. (10 cm).

In addition to shielding and basic-access control, the chip has more than 50 security mechanisms, including sophisticated computing methods for encrypting data, to help ensure that personal data remains private. Security mechanisms also include active protective shields on the surface of the chip and sensors that help prevent unauthorized people from being able to read the contents of the chip.

—by Vinod Kataria, *EDN Asia*

▶**Infineon Technologies**, www.infineon.com.

New US passports will integrate chips from Infineon Technologies.

To avoid the need to develop with two (or more) different sets of development tools, select a single family of MCUs, including both USB and low power devices, so that firmware development across the system uses a single tool chain. If possible, it is also advantageous to select the MCU family and the RFIC from the same vendor, because the protocol firmware will be available for these MCUs – eliminating the need to port the firmware from another MCU. However, just as protocol is a key criterion for selecting the RFIC, so the features and quality of the development tools are an essential part of selecting the MCU. An Integrated Development Environment (IDE), In-Circuit Emulator (ICE) and source-level debugging (if developing in "C") are essential for fast and effective firmware development – even if the code size will be small. Most firmware engineers have written custom RS232 debugging output firmware, but with the widespread availability of high quality IDEs and ICEs the old "roll your own" approach to debugging is no longer competitive.

The Benefits of In-System Reprogrammability

Selection of a Flash-based rather than One-Time-Programmable (OTP) or Mask ROM MCU will help you throughout the development process by enabling In-System Reprogrammability (ISR). Making a firmware change during development and testing no longer means unscrewing the enclosure, removing the PCB, and then desoldering the MCU. With a Flash MCU and a well-positioned ISR header (for example inside the battery compartment) uploading code changes is easy – you can even upgrade prototypes in the hands of beta testers by simply emailing them a new hex file, rather than having to send out a costly series of new prototypes. Some USB MCU vendors even support reprogramming over USB – eliminating even the need for a special programmer during development of the RF dongle.

Another consideration is the level of support you can expect from your chosen RFIC and MCU vendors; do they have a portfolio of application notes and reference designs to get you started? Is there a knowledgeable Field Applications Engineer (FAE) in your area? How much do the MCU vendor FAEs know about RF? Selecting a single vendor for both RFIC and MCUs with a worldwide support network will ensure your success if you run into problems.

Navigating Manufacturing Test

One important area often overlooked by first-time developers of 2.4-GHz products is manufacturing test, along with the related aspects of regulatory compliance. A single poor solder joint on one of the components between the RFIC and the antenna, or even a simple problem with a decoupling capacitor, could cause a change in the RF spectrum of your product, causing it to violate regulatory compliance standards even though it still passed a simple, functional final manufacturing test. Some form of radiated testing during manufacturing is essential for preventing the shipment of non-compliant devices that result from minor manufacturing defects — this will require the development of special test firmware. The conventional approach to radiated testing is to test in a screened room with an operator checking the transmitted spectrum using a spectrum analyzer connected to an antenna. However, this approach is costly, both in labor and the cost of the screened room facilities. An equally effective, but dramatically lower cost solution is to use a small screened test box lined with RF-absorbent foam and a Bit Error Rate (BER) tester. By performing BER testing close to the limit of sensitivity it is possible to detect any manufacturing defects in the RF subsystem. Some RFIC manufacturers provide a complete reference design for this approach, eliminating the need for you to begin from scratch; all you need to do is integrate the provided test firmware into your code.

One option is to include this test firmware in the main code, with entry to the test mode being triggered by a special button press sequence during and immediately after power-on. However, if you are using an ISR-capable Flash MCU, the burden of this firmware on the limited available memory can be eliminated by programming the product with the special test firmware image during manufacturing, and then replacing it with the final product code after RF test.

As we have seen, careful consideration of the system-level challenges when selecting key components can ease the design challenges facing the designer of wireless input devices. However, these lessons go far beyond this specific application – selecting programmable solutions with comprehensive development tools and support is a key first step to success for any new product development. ■

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Whether you're upgrading your user interface with capacitive sensing technology, or adding state-of-the-art biometric security to a thumb drive, Cypress PC Peripheral solutions offer the following benefits:

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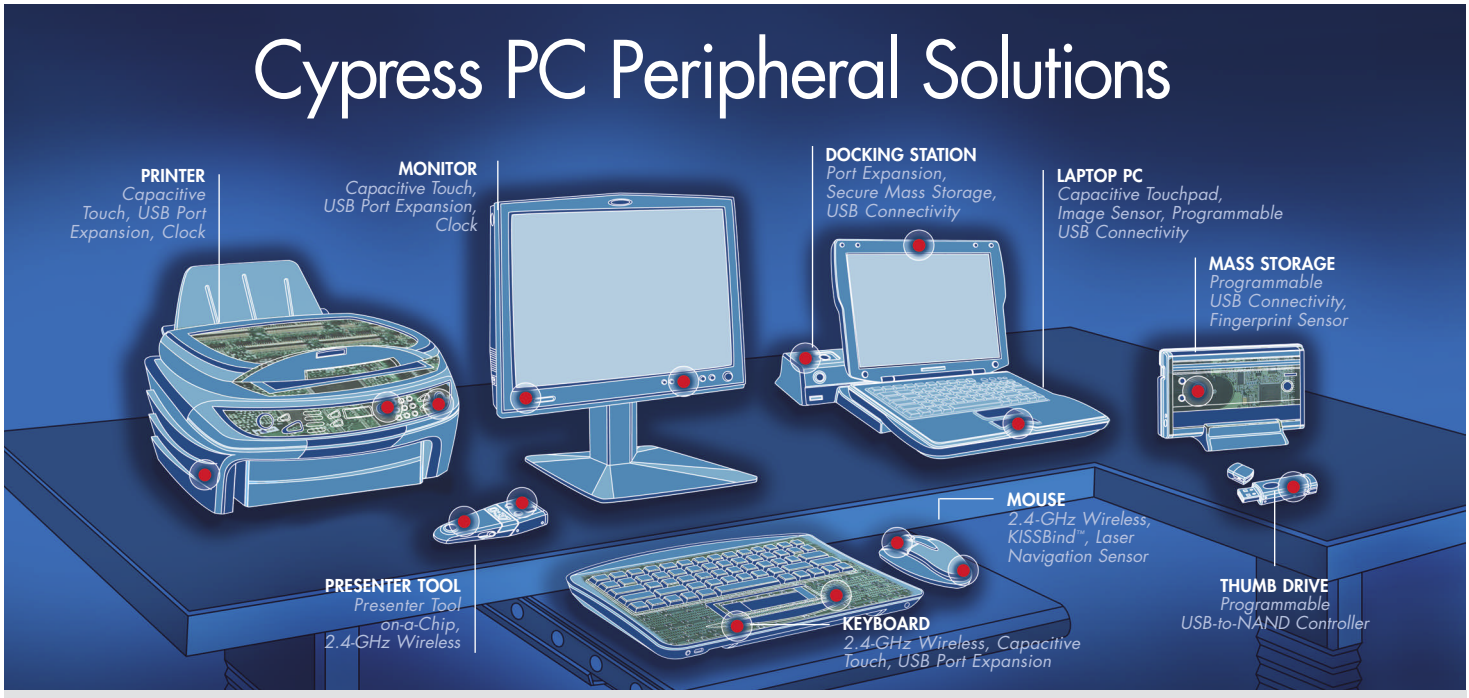

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Addressing the System-Level Challenges of Wireless Input Devices

by David Wright, Member of the Technical Staff, Cypress Semiconductor Corp.

The article below, one in a series of design solutions pieces for EDN readers, explores some of the challenges facing designers of wireless PC Peripherals. For access to Cypress's library of extensive staff-written contributed articles, visit us at ***www.cypress.com/techlibrary.***

The popularity of wireless input devices (mice, keyboards, gamepads, etc.) continues to grow, but designing with these products generally involves a significant increase in complexity compared with their "wired" predecessors (usually USB).

Which RF technology will you choose? How to sort out options related to the MCU and its development tools. Will you opt for programmable or fixed-function devices – for standard ICs or proprietary solutions? Finally, if you are designing with 2.4-GHz wireless technology, how will you handle the manufacturing test phase where a single poor solder joint can throw your system out of whack and bring on a regulatory violation?

Let's take a look at some of the more common pitfalls in the design process and some basic ways to avoid them.

Picking the Radio

The first decision confronting you is the choice of RF technology. The various 2.4-GHz RF technologies are rapidly becoming the solution of choice for wireless PC peripherals and consumer products because a single product design may be sold worldwide – unlike most earlier RF technologies which had to navigate a maze of varying government regulations. Within the 2.4-GHz offerings, you must choose between a standard (such as Bluetooth, Zigbee, 802.11) and a proprietary system. None of today's standards include both low latency and long battery life, which are critical specifications for wireless input devices. Therefore a proprietary solution is usually the best choice. However, this does not mean designing and testing a protocol from scratch – most vendors of 2.4 GHz RFICs offer fully developed and thoroughly tested protocols for use with their devices. Because the 2.4-GHz ISM band is shared with a host of other devices (such as WiFi and cordless phones), you should pay particular attention to the device's interference immunity to avoid erratic performance characteristics.

Selecting the MCU

Once the choice of RF technology has been made, the next decision is microcontroller selection. A wireless input system typically has a low power MCU in each of the devices, and a USB MCU in the "bridge" or "dongle" as shown in figure 1.

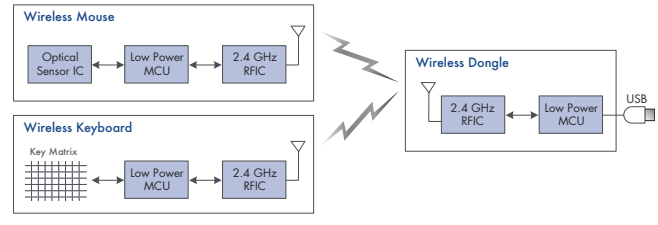
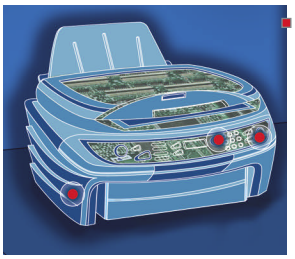


Figure 1. Wireless Input System and Major Components

continued on page 4 >>

CYPRESS PERFORM

PSoC For Printers



PRINTER

Capacitive Touch Sense, Resistive Touch Sense, USB Port Expansion, Clock

Cypress offers design solutions for all levels of printer systems, from low-end consumer inkjet printers to high-end multi-function printer/copier/scanner systems. Cypress's Programmable System-on-Chip™ (PSoC®) mixed-signal array performs a variety of functions in printers, including motor control, capacitive touch-sensing replacements for buttons and switches on the control panel, and checking ink levels in printer cartridges.

- *Capacitive sensing is an elegant, cost-effective replacement for buttons and switches on a printer's control panel. Using no moving parts, capacitive sensing increases the durability and effective lifespan of the equipment with no added cost. Cypress's PSoC-based CapSense technology brings a flexible architecture, system integration and cost reduction to interface applications.*
- *Motor control – precisely controlling the cartridge position for the highest image quality while ensuring fast operation – is a crucial capability in a printer. PSoC's flexible, configurable analog and digital blocks enable the construction of motor controllers that deliver precise, reliable results.*
- *A single PSoC chip can dynamically reconfigure itself to implement both cartridge-level detection (reminding the user when ink levels are low) and cartridge verification (authentication of a product approved by the manufacturer).*

Printer Selector Guide

Part No.	Analog	Digital	Flash	RAM	HW Comm Bus
CapSense					
CY8C21X34	2E	4	8K	512 bytes	12C
CY8C24X94	6	4	16K	1K	12C
Motor Control					
CY8C27X34	12	8	16K	256 bytes	12C
CY8C24X23	6	4	4K	256 bytes	12C
CY8C21X23	2E	4	4K	256 bytes	12C
Ink Level Detection and Cartridge Verification					
CY8C21X23	2E	4	4K	256 bytes	12C

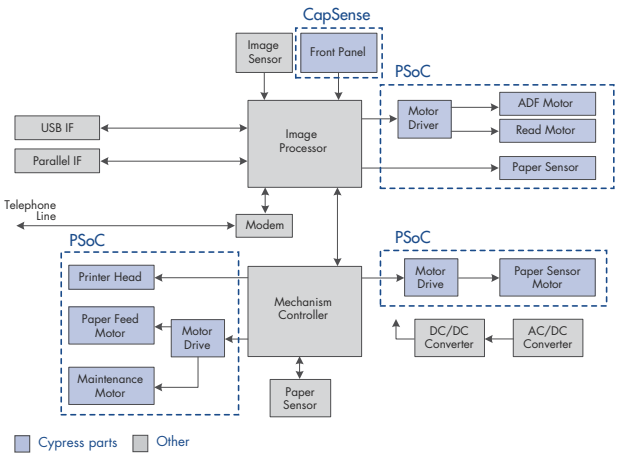
FEATURES

- Easily implemented capacitive sensing units, such as buttons, sliders, touchpads, or proximity detectors using PSoC CapSense
- Configurable PSoC architecture supports multiple sensor types and other functions in a single device
- Configurable analog and digital blocks allow implementations of ADCs, DACs, filters, amplifiers, comparators, PWMs, counters, etc.
- SPI, UART and I²C interfaces to communicate with printer controller.
- No proprietary software dependencies while reusing subsystem IP across platforms
- Dynamic reconfigurations
- User configurable pin-outs
- Storage of usage statistics in EEPROM, including
  - Ink level
  - Number of cleaning cycles performed
  - Time of installation of the ink cartridge
  - Accumulated installation time of the cartridge
  - Model name of the printer in use

BENEFITS

- Appealing, product differentiating user interface with CapSense technology
- Reduce the number of discrete components with PSoC integration
- Reduces PCB size and system cost
- Add system capabilities with no added hardware cost
- Reduces hardware design complexities

INK JET PRINTER BLOCK DIAGRAM



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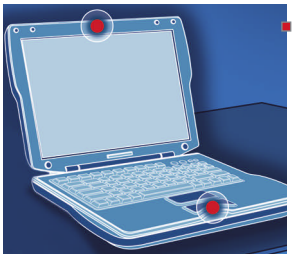
Application Notes

- AN2292 – Layout Guidelines for PSoC CapSense
- AN2229 – Motor Control – Multi-Functional Stepping Motor
- AN4002 – Calculating Battery Life in WirelessUSB Systems

Reference Designs

- CY4602 – High-Speed USB 2.0 4-Port Hub
- CY4636 – WirelessUSB LP™ Keyboard-Mouse Reference Design Kit (ver. 1.0)
- CY4651 v1.2 – Cypress and AuthenTec Reference Design for Biometric Security in External USB Hard Disk Drives
- CY4651, CY4661, CY4671 – Reference designs for Biometric Security in External USB Hard Disk Drives with AuthenTec, UPEK and Symwave
- CY4655, CY4665, CY4675 – Reference Designs for Biometric Security in USB Flash Drives with AuthenTec, UPEK and Symwave
- CY4684 – USB Video Class (UVC) Compliant Reference Design for PC Cameras

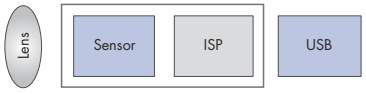
PC Cameras



PC Camera
Integrated PC Camera using USB, Capacitive Touch

Cypress is the industry-leader in USB with more than a half-billion USB controllers shipped to date. Recently, designers have begun to use USB as an internal data bus, enabling the integration of webcams in notebook PCs, Media Center PCs and LCD monitors. The USB 2.0 standard provides throughput of up to 24 Mbytes isochronous and 40 Mbytes bulk, enabling videoconferencing and other new applications built around high-speed data transfer capabilities. Ask for a demo today.

EMBEDDED WEBCAM BLOCK DIAGRAM



FEATURES

EZ-USB FX2LP™ (CY7C68013A)

- High-Speed USB interface complies to USB 2.0 specification
- WHQL Certified
- Smallest footprint - 5 mm x 5 mm VFBGA
- Lowest power for maximum battery life – 100 uA standby, 50 mA active
- High throughput maximized for video applications - 24 Mbytes (isochronous), 40 Mbytes (bulk)
- Reference design available in 2H2006
- USB Video Class (UVC) compliant reference design

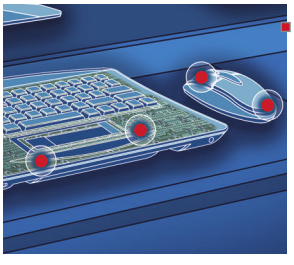
BENEFITS

- Complete video solution for quick time to market
- 1.3 MP/15 fps, VGA/30 fps video quality
- 1.3 MP image capture quality
- Seamless integration between SoC and USB greatly reduces design effort/cost
- Microsoft Video Class Driver compliant
- Plug and play with Microsoft XP operating system and beyond

PC Camera Selector Guide

Name	Data Throughput	Video Quality	Power Consumption
CY7C68013A	24 Mbytes (Isochronous) 40 Mbytes (bulk)	1.3 MP/15 fps, VGA/30 fps	100 uA standby 50 mA active

Human Interface Devices (HID)



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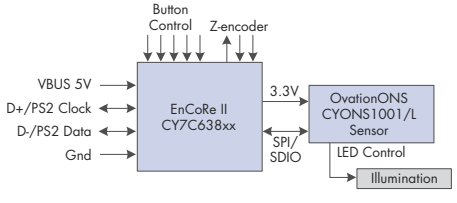
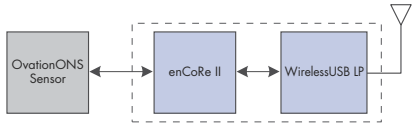
WIRED MOUSE BLOCK DIAGRAM



WIRELESS OPTICAL MOUSE BLOCK DIAGRAM



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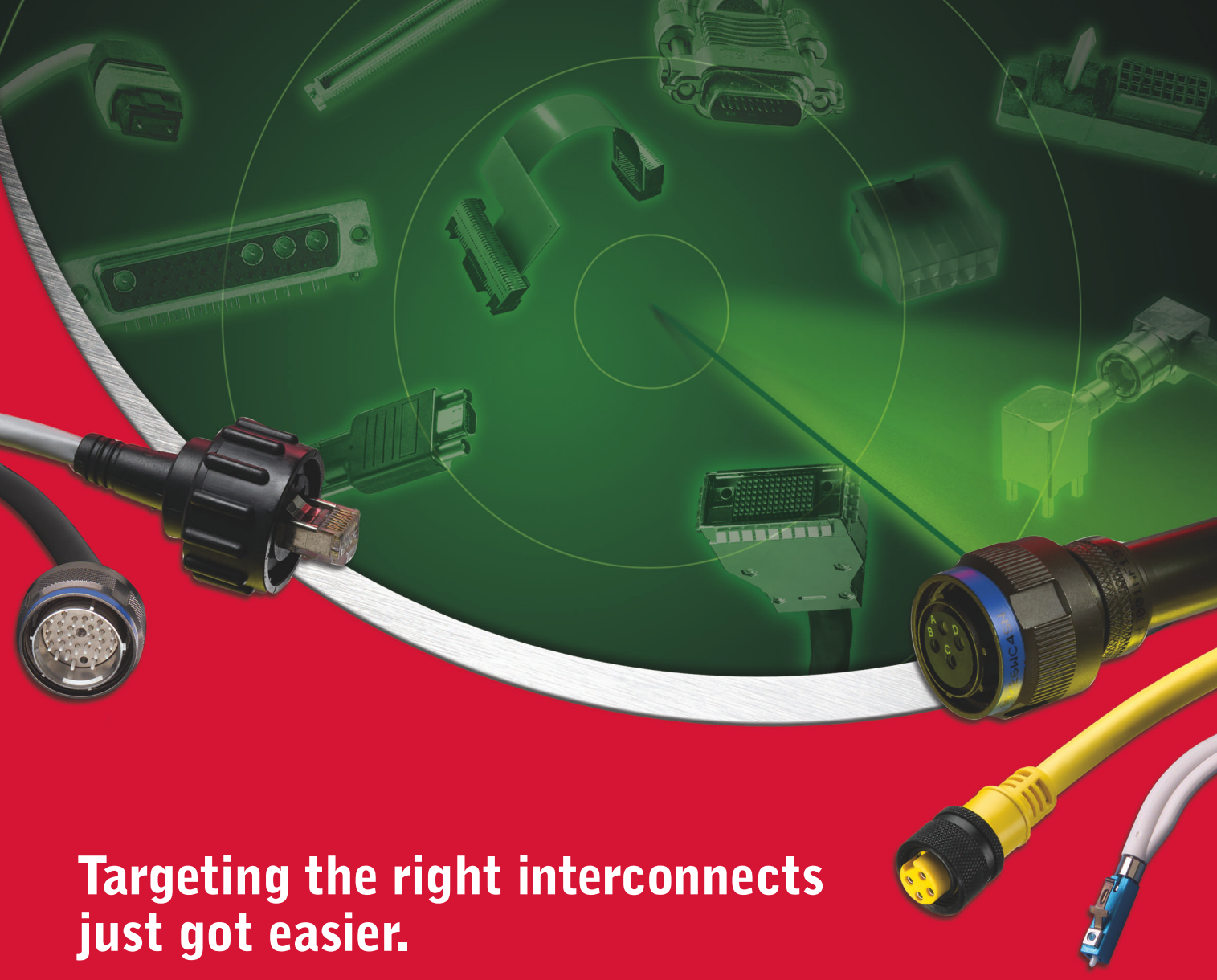
OvationONS Laser Sensor

- Highly integrated solution for mouse manufacturing simplicity
- High performance with low power

HID Selector Guide

Name	Connectivity	Data Rate	Core	Other
enCoRe II	Low-Speed USB	1.5 Mbps	M8™ 8-bit MCU	4K–16K Flash
enCoRe III	Full-Speed USB	12 Mbps	M8 8-bit MCU	16K Flash
WirelessUSB Radios	2.4 GHz Wireless	Up to 1 Mbps	DSSS, GFSK, Modulated Radio	Up to a 50 meter range



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Megabit DRAMs led PC boom, despite claims that they were "too capacious"

Toshiba (www.toshiba.com) led the procession of DRAM vendors to the 1-Mbit level in the mid-1980s, although, as a 1996 *EDN* article indicates, the jury was out on when the devices would find mainstream use. (For the entire article, see "Dynamic RAMs," *EDN*, Feb 20, 1986, pg 134 or go to www.edn.com/060914milestones.) Typically, the move to higher density, 1-Mbit devices would wait for the cost per bit to near what 256-kbit devices offered. But the 1986 article also questioned the applications that could use 1-Mbit DRAMs, especially in the 1M×1-bit organization that first came to market. The article noted that expected 256k×4-bit products might prove more popular.

We presume that the author of that 1986 article was a fairly bright fellow, but surely he failed to recognize just how quickly the PC would become a memory hog and how the megabit and higher density DRAMs would prove almost as important as fast processors in enabling compelling PC applications.

As it turned out, the ×4-bit parts would find use only in niche embedded-system applications. The move to SIMM (single inline memory modules), which the author ignored, was already under way. Indeed, that issue of *EDN* carried ads for SIMMs. Molex (www.molex.com) had developed the SIMM socket working with Wang, which developed the first SIMMs for its dedicated word processors. Indeed, Wang would wind up in lengthy litigation with Mitsubishi (www.mitusubishi.com) over SIMM intellectual property. Those first SIMMs were ×8- or ×9-bit modules, and IBM (www.ibm.com) would be first to develop ×32- and ×36-bit modules for the PS-2.

The 1986 article is also interesting in its discussion of process technology. Most DRAM players believed that NMOS DRAMs would continue to dominate. Those thoughts are understandable because CMOS was then more expensive and required more transistors per chip. But memory is where Moore's Law really shined, and CMOS and low power would ultimately rule in memory and everywhere else.EDN

02.20.86

FROM THE VAULT

Dynamic RAMs

THE HIGH COST AND 1-BIT-WIDE ORGANIZATION OF 1M-BIT DYNAMIC RAMS ARE NOW LIMITING THEIR USE. NEVERTHELESS, PRICES COULD FALL TO $20 BY YEAR'S END, AND 256k 34-BIT VERSIONS ARE EMERGING.

Traditionally, spec'ing a dynamic RAM involved nothing more than process technology, memory capacity, organization, and access-time requirements. The emerging 1M-bit devices, however, will complicate the specification process. Although every manufacturer of 1M-bit commodity dynamic RAMs will offer parts with similar operational characteristics (CAS-before-RAS refreshing and page-mode addressing, for instance), you'll have to consider such factors as cell-capacitor architecture, access mode, price trends, producibility, packaging, and testing, in addition to the CMOS-versus-NMOS issues.

Furthermore, consider whether or not a 1M-bit part best suits your application. The 256k-bit chip will have a long life and can save you money in some designs. In addition, devices with lower capacities offer features that won't be available in 1M-bit parts for several years. For example, several manufacturers offer less dense dynamic RAMs that have access times superior to those of 1M-bit devices. Inmos, for instance, offers the IMS2800 256k×1-bit CMOS dynamic RAM with a 60-nsec access time, and Visic offers the V64H1 64k-bit hierarchical random-access memory (HRAM), which operates like dynamic RAM but features a 35-nsec access time.

DON'T COUNT OUT THE US VENDORS

Recently, dynamic RAMs have made the evening news on a regular basis. Several US companies have dropped all or a portion of their dynamic-RAM business. Japanese companies appear to be ready to attack the US market for 1M-bit devices. Toshiba began shipping production 1M-bit parts in October 1985, and Fujitsu and Hitachi plan to ship production quantities this quarter. But several domestic companies plan to be strong contenders: AT&T, Texas Instruments, and Micron Technology are sampling 1M-bit parts or plan to sample them this quarter.

In addition, once some standards issues are settled and the 1M-bit chips are well into production, expect to see niche versions of the part. For example, Advanced Micro Devices plans to concentrate on sub-80-nsec RAMs with 256k×4-bit organizations, which would be useful in the communications industry. The company also plans to develop 1M-bit video RAMs.—*Feb 20, 1986*


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BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Stacking up

Advances in IC packaging and back-end manufacturing processes that take advantage of 3-D structures are beginning to blur the line between fabrication and packaging technologies. That the result could substantially increase the IC's I/O density is an understatement: IBM reports results that suggest that an exponential improvement in I/O density is possible with 3-D-IC integration (**Reference 1**).

With the widespread adoption of surface-mount-assembly methods in the 1980s, package-to-board interconnect density took the important step from through-hole technology's traditional 100-mil lead pitch to a 50-mil pitch. Though perhaps a quaint perspective now, this move at the time seemed like a bold one because the surface-mount components did not mechanically interlock with the board to ensure their alignment. As assembly equipment, alignment methods, and surface-mount-soldering technologies continued to improve, so did package I/O density, leading to the use of the now-ubiquitous BGA (ball-grid array). (Students of packaging history will note that IBM developed an early form of BGA in the 1960s for mounting transistors in the System 360. Such mounting methods, however, did not enjoy widespread use for three more decades.)

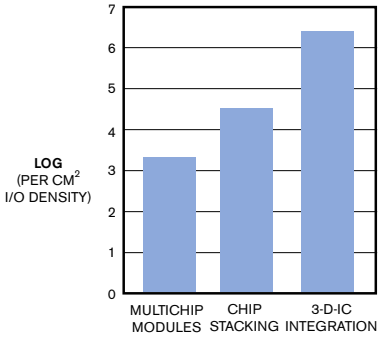

Figure 1 A stacked-die technology, 3-D-IC integration, increases density over multichip modules and chip stacking.

During this same historic interval, the density at the die-to-package interface increased, as well, reflecting the growth in functional density that CMOS-fabrication-process scaling facilitated. One innovation, the MCM (multichip module), allowed manufacturers to combine chips in a single package—an economic construction reminiscent of comparatively expensive chip-and-wire hybrids. As with hybrids, MCM assembly mounts dice in a planar arrangement on a substrate. Unlike hybrids, MCMs generally use organic packaging and leave passives as external components. Traditional wire bonds can make the chip-to-package connections, or, in the case of high-I/O-count modules, those interconnects can take advantage of flip-chip technology, with I/O pitch in the 150- to 200-micron range. These modules reach interconnect densities on the order of 10^3 I/O per cm^2 (**Figure 1**).

So-called SIP (system-in-package) technologies replace the MCM's planar layout with die stacking. Die stacking provides a rare opportunity in assembly technologies to construct shield plates, which are useful for shielding sensitive nodes in high-gain analog-signal chains from noisy digital sections in mixed-signal modules (**Reference 2**). The vertical structures also facilitate shorter interchip connections for better high-frequency performance than MCMs provide. Low-I/O-density functions can use bond wires for chip-to-chip and chip-to-package connections and still reduce the finished product's footprint to less than that of an equivalent MCM. In high-density modules, area-array interconnects feature I/O pitches of approximately 50 microns and connection densities greater than 10^4 I/O per cm^2.

The IBM paper describes a stacked-die technology, 3-D-IC integration, that exploits silicon through-vias and attains a 6-micron pitch and 10^6 I/O per cm^2. The silicon-on-silicon technology provides interconnection bandwidths as high as 6 GHz and avoids differential coefficients of thermal expansion of adjacent layers for mechanical robustness.

One challenge to high-speed, high-density modules is decoupling. The 3-D-IC integration provides for integrated bypass capacitors constructed on silicon-interposer layers on the chip side of the chip-to-board stray inductances.

Thermal plates on the top can conduct heat from the active devices to the package's lid. Such 3-D-cooling structures can further enhance the package's ability to support both speed and functional density. EDN

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2 Israelsohn, Joshua, "Newton's chips: low-g accelerometer ICs," *EDN*, Oct 28, 2004, pg 65, www.edn.com/article/CA472836.

Joshua Israelsohn is director, technical information at International Rectifier Corp. You can reach him at edn-joshua@mindspring.com.


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BY HOWARD JOHNSON, PhD

Voltage-regulator droop

The circuit model in **Figure 1** captures the important low-frequency behavior of most voltage regulators (**Reference 1**). Parameters C_2, R_2, and L_2 represent a typical bulk decoupling-capacitor array. To model the response below 100 kHz, you can set L_2 to 0. Parameter R_1 models the regulation resistance, or stiffness, of a small switching-regulator module. Parameter L_1 models the response time.

Now try something outrageous. Add series resistance to the regulator output, effectively increasing the value of R_1.

When the load draws current, the new, larger value of R_1 increases the droop measured at V_{CC}. That scenario sounds bad, but in some special circumstances, it is actually good for your circuit.

Figure 2 shows the regulator-voltage response for values of R_1 from 3 to 12 mΩ. The circuit is subject to an 8A step load with a maximum dI/dt of 2.5A/μsec. The plot shows the load current at the bottom and the collection of response curves at the top. It offsets each curve horizontally to visually separate them.

Concentrate on the red waveform (minimum value of R_1). Beginning from rest at Point A, the V_{CC} output sits at its nominal, midlevel value. When the load turns on, V_{CC} responds with a downward glitch.

Only components C_2 and R_2 limit the initial amplitude of this glitch, because the regulator can't respond instantaneously; it takes a few switching cycles to respond.

Once the regulator wakes up, it drives the voltage back to a new operating Point B. The sluggish response of the regulator mimics the action of an inductor, which is why **Figure 1** makes such an effective model.

When the load switches off, the response pops back high at Point C. (Inductors do that.) The overall peak-to-peak response of the red waveform equals nearly twice the amplitude of the initial glitch.

Now, increase R_1 to 0.012Ω and reapply the load. The black waveform goes down and stays down, displaying more long-term droop because of its larger series resistance. When the load cuts off, the positive glitch that inductor L_1 causes begins at a lower level. Beginning lower, this glitch does not reach as high as the glitch on the red waveform. As a result, you obtain the smallest peak-to-peak response with R_1=0.012Ω.

If you use this method, offset the resting voltage of your regulator toward the high end of its range to best center the overall step-response waveform.

Some switching regulators let you lower the gain of the control loop, effectively increasing the regulation resistance, R_1, without dissipating additional power. This cool trick does not work for linear regulators.

Whatever you do, beware of the tolerances associated with all components in this circuit. Do not design something so tricky and intricately balanced that small changes in component values throw the system out of whack.EDN

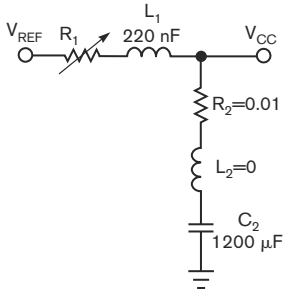

Figure 1 Some regulators provide adjustable droop.

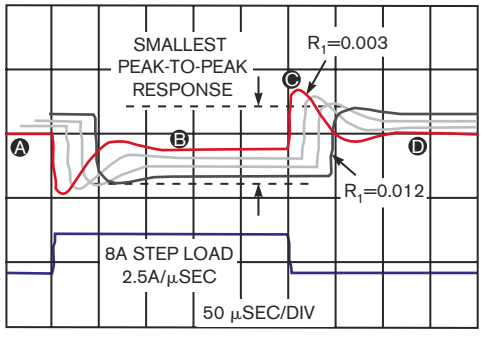

Figure 2 Adjusting R_1 changes the peak-to-peak response.

REFERENCE

1 Johnson, H, "Voltage-regulator model," *EDN*, Aug 17, 2006, pg 22, www.edn.com/article/CA6360320.

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Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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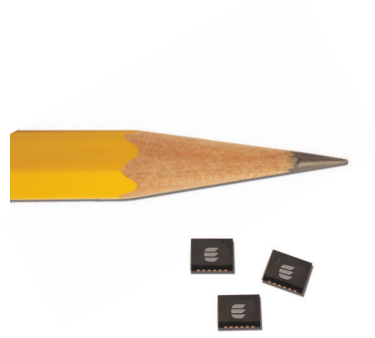

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Perceptions and realities

DANIEL VASCONCELLOS

In the late '60s, I was a newly minted EE graduate from the University of Toronto. The job market was hot, and I was offered two jobs: One paid well as a "catalogue jockey" at the CBC (Canadian Broadcasting Corp), and the other, at Ferranti-Packard, paid poorly but included real design work. I took the second job, because it sounded like a better learning experience.

As a new engineering graduate, I was tremendously skilled at solving differential equations but had no idea how to build anything. Alert to talent, the manager made me responsible for the design of a regulated power supply for a digital measuring instrument. This era predated CMOS, LEDs, IC op amps, and MSI (medium-scale integration). Digital circuits used bubble-gum DTL (diode-transistor logic), and the displays were Nixie tubes. The circuitry used a lot of power.

Switching power supplies were still mil-spec exotica, so the regulator was a discrete-transistor series-regulator design. My calculations indicated that the series regulator would dissipate many watts of power and require a massive heat sink. But the large heat sink was a mechanical inconvenience, and it seemed intuitively obvious that the transistor couldn't get as hot as my calculations predicted. I specified a smaller heat sink and hoped for the best.

I threw the design over the wall to the prototype technicians and assumed it would find its way into production. A few days later, a contingent of technicians visited me in my cubicle. "We'd like to show you your power supply," they said. I should have known something was wrong; they seemed uncharacteristically gleeful.

In the lab, my beautiful power-supply design resided under a large pile of fire retardant. "Your supply caught fire," they told me. "We had to use the fire extinguisher."

I pronounced myself an idiot, to which there was general agreement and more merriment. I retreated to my desk and slide rule. This time, I paid more attention to my calculations. The new design, which included a much larger heat sink, ran at a reasonable temperature.

AND NOW IT OSCILLATED

In my then-limited experience, it sometimes helped to turn an error amplifier into an integrator. Not in this case. After a day of fruitless tinkering, one of the senior engineers suggested looking at the loop gain and phase curves. I'd studied control-system stability at the university but in a very theoretical manner. It was a major leap of faith to think those tools could apply to this problem. After much slide-rule analysis, the Bode plots suggested that a lag-lead network would do the trick. Without much hope, I soldered in the appropriate combination of resistor and capacitor. To my astonishment, the supply was stable. Such moments are the delights of engineering: Pages of calculations predict some result, and the prediction turns out to be correct.

From then on, I put much more emphasis on careful, thorough design work. As I came to realize, design calculations are what mathematicians call a necessary but insufficient condition. If a design does not work on paper, then it is irresponsible to expect that it will work in practice. And for the design to be useful, it has to be thorough—heat sink and gain margins included.

There's more to it than the design, of course. Years later, an academic engineer suggested to me that an engineer's job is done when the simulation runs correctly. But, as every practicing engineer knows, the theory may be incomplete, the models may be inaccurate, and external factors may confound correct operation. So, bench testing is another necessary but insufficient condition. It doesn't replace careful design. EDN

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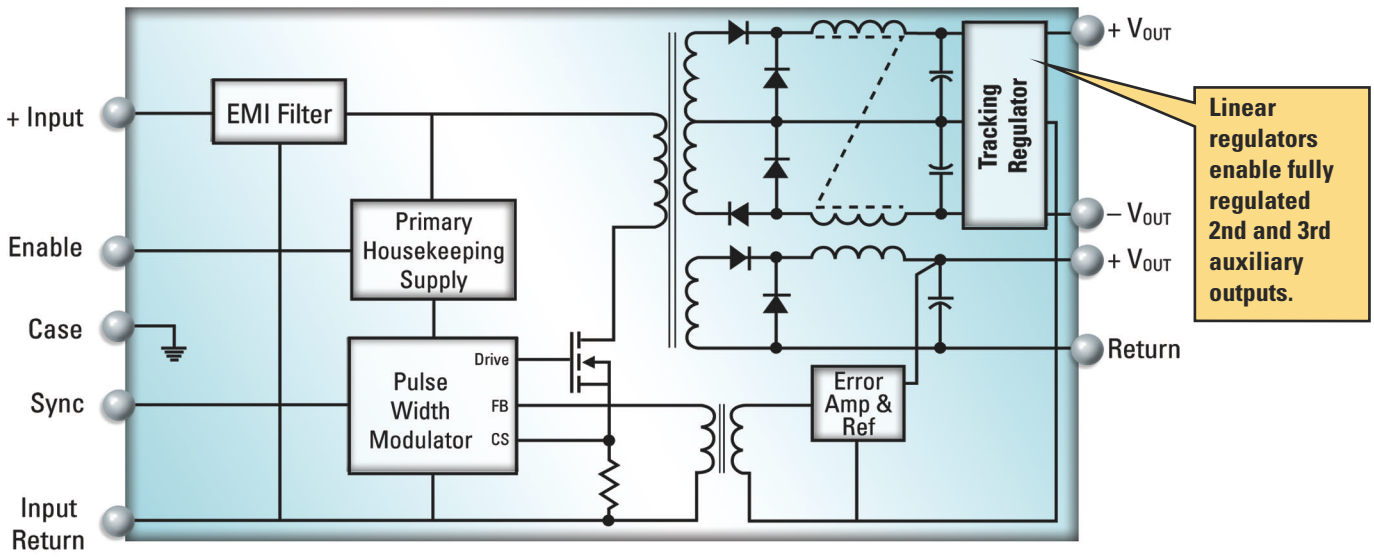

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Dimensions (in.)
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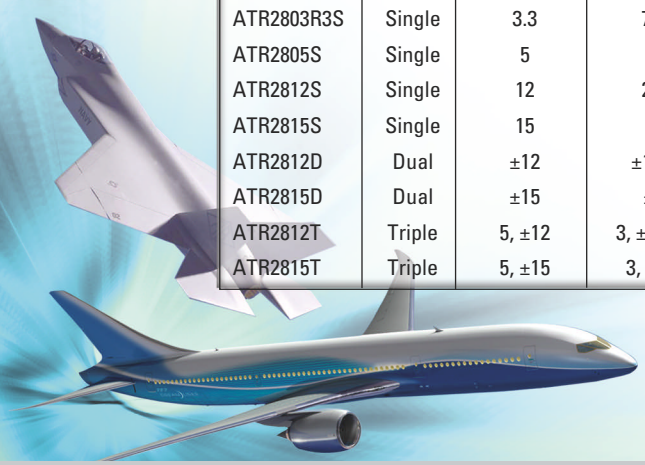

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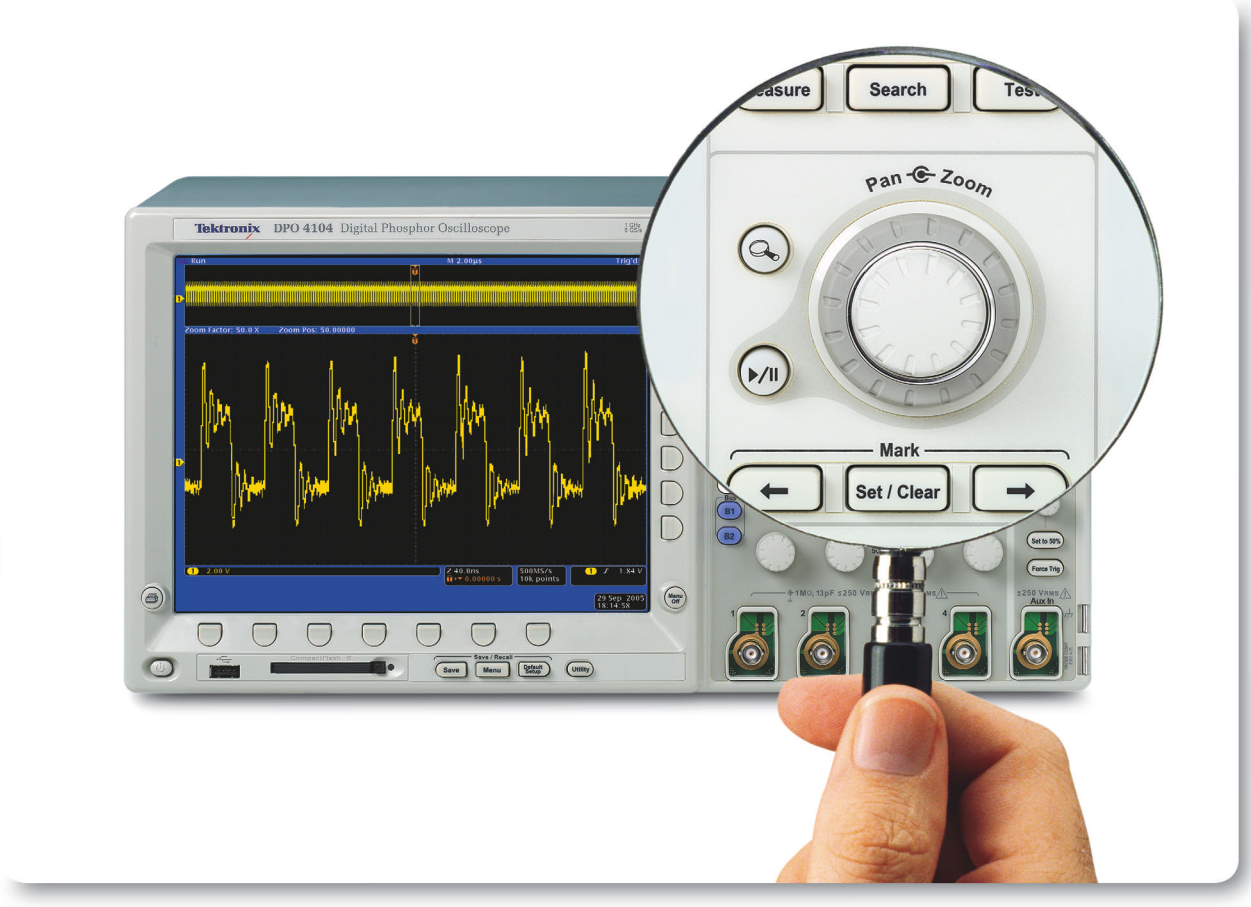

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SDR goes to war

BY NICHOLAS CRAVOTTA • CONTRIBUTING TECHNICAL EDITOR

THE JTRS IS WORKING TO BRING INTERCHANGEABLE SDR TO THE MILITARY. BUT WILL IT BE GOOD ENOUGH FOR COMMERCIAL APPLICATIONS?

SDR (software-defined radio) is not a new technology. The industry has in the past made attempts to implement SDR, but these efforts have fallen short. What has sparked recent interest in SDR is the rise of innovative hardware and software technology that appears to offer enough flexibility, performance, and power efficiency at a price the market can bear. For example, wideband converters are now available that operate over a wide range of frequencies and can process incoming waveforms based on a specific bit resolution, and high-frequency processors can work with signals directly, eliminating IF (intermediate-frequency) stages and reducing cost.

The appeal of SDR stems from an understanding that moving to a single hardware platform that can handle multiple radio technologies will not, as you might expect, cost more than individual radio designs that target the lowest cost for an application. The hope is that a versatile platform will introduce significant economies of scale, increase radio functions, and release the military from the bondage of proprietary implementations.

The cost efficiency of SDR derives from the premise that maintaining a single radio platform is less expensive than managing multiple platforms. Certainly, ASICs offer a cost advantage in high-volume applications over FPGA and DSP implementations. However, when you consider multiple platforms, the continually decreasing cost of FPGAs and DSPs and the reusability of software can offset the cost of developing and maintaining multiple ASICs.

ECONOMIES OF SCALE

The drive behind SDR in both military and commercial applications is to reduce cost. The military seeks to achieve this goal by attempting to reduce the total number of radios that an individual must carry. From a commercial perspective, SDR focuses less on supporting multiple radio technologies than it does on reducing design and development effort, increasing radio robustness through comprehensive upgrades, and enabling next-generation architectures to reuse IP (intellectual property) by building on previous implementations.

Currently, the military wants to support more than 30 protocols. These protocols use a number of both secure and nonsecure waveform types. Driving the promotion and advancement of SDR for military applications is the JTRS (Joint Tactical Radio System). The JTRS' SDR efforts aim to promote the availability of off-the-shelf hardware and software components that enable a single implementation to handle

AT A GLANCE

- SDR (software-defined radio) promises to enable transparent interchangeability of both hardware- and software-radio components to simplify radio development and deployment.
- Standardization efforts from the military focus on the SCA (Software Communications Architecture) framework.
- The SCA framework has thus far failed to successfully abstract specialized hardware resources, such as FPGAs and DSPs.
- Commercial SDR applications focus on innovation and low cost rather than total interoperability, limiting the SCA's value in commercial applications.

multiple protocols' waveforms that also target the best power, performance, and cost.

The ability to support multiple protocols holds less value in the commercial world than in the military world. Often, less than a handful of protocols is competing within an application space. Two primary nonmilitary applications—cellular and safety—focus on SDR technology. In the cellular world, base stations that can support multiple radio technologies—such as both GSM (Global System for Mobile communications) and CDMA (code-division multiple access)—expand the capabilities of the cellular network and increase potential operating revenues. For safety applications, for example, service groups such as police and fire personnel use different radios; a universal radio would eliminate the need for these individuals to carry multiple radios to coordinate efforts.

These perspectives significantly alter how these industries have approached SDR. For example, a world phone that can operate on any band would have limited usefulness and an even smaller market share. The military seeks consolidation, whereas the commercial world seeks design simplification and efficiency.

SDR'S PROMISE

The ultimate goal of SDR is to create a radio in which frequency, IF, baseband, modulation, protocols, hopping frequency, and so on are programmable. A typical radio implementation fixes many of these characteristics, limiting the radio. True SDR strives to make it possible to modify any of these parameters.

Current implementations of SDR are still a long way from the ideal universal radio that marketing managers envision. Today, most radios use ASICs to implement a radio, and front ends target particular applications. Generic front ends covering multiple bands and frequencies that you could modify using software are still not here. Rather, operators must either send the radios back to the factory to reprogram the waveforms or, more appealing to those in the field, swap out an RF module on their own.

Another cost savings that SDR enables is the ability to dynamically reconfigure radio resources to match current system needs. Consider a military or commercial base station populated with a single type of reconfigurable board. You could configure this base station to support waveform allocations through software alone. For example, you could allocate the resources of various boards in a base station to handle 20 channels of Waveform A and 20 channels of Waveform B. In the event of equipment failure, such as a board that supports 10 channels of Waveform A becoming disabled, you could reallocate the remaining channels appropriately to support a 20/10, a 15/15, or another mix appropriate to the application and current waveform usage.

A fully dynamic and reconfigurable radio offers many benefits besides support of multiple bands. For example, a radio could use FEC (forward-error-correction) techniques to match the terrain in which the radio is operating. Additionally, reconfigurable radios can immediately take advantage of innovation, such as a more efficient waveform implementation or a robust security mechanism.

SDR also promises to minimize development time, as designers can reprogram a radio if a problem arises in the field or a protocol changes. For example, although protocols themselves may stay static, algorithms, waveforms, and modulation schemes continue to improve over time. With an SDR-based architecture, you can take advantage of these improvements and innovations without redesigning the radio.

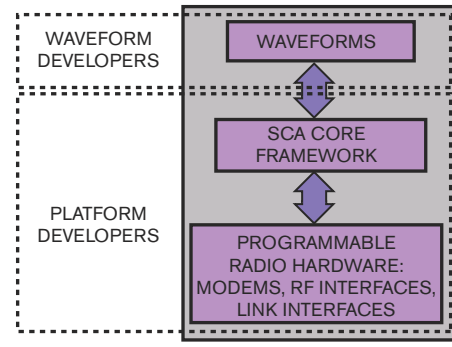

Figure 1 The SCA framework is the glue between hardware and software. Its goal is for any SCA-compliant waveform to operate on any SCA-compliant radio hardware. CORBA—the middleware layer sitting between the operating system and SCA framework—transmits data between software objects over a software bus. Implementing CORBA on specialized hardware such as a DSP or an FPGA without a substantial performance penalty is not a straightforward task (courtesy Pentek).

THE SCA FRAMEWORK

The keystone of the JTRS' mandate to promote SDR in military applications is the SCA (Software Communications Architecture) framework. The JTRS is developing this framework to break the link between hardware and software, which in turn will break the hold that proprietary implementations have on the military. The system implements functions using a radio's available hardware and software resources, which may differ from vendor to vendor.

The SCA sits above the operating system and is the glue between hardware and software (**Figure 1**). The goal is that any SCA-compliant waveform will operate on any SCA-compliant radio hardware. Such hardware/software interoperability is a major consideration in military applications; it is not trivial to swap out a radio in an F-15 fighter jet. SCA promises to effectively eliminate the difficulty of supplying new radios and upgrading any deployed radios in the field.

Today's SCA framework supports portability of waveforms a few steps shy

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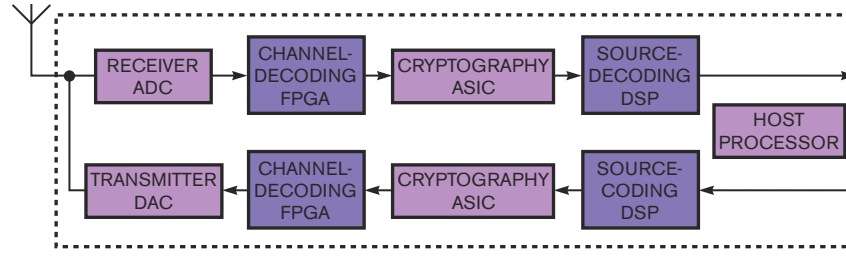

Figure 2 Although the SCA framework supports portability of waveforms, it primarily targets general-purpose processors. To achieve sufficient performance and cost efficiencies, however, most designs today employ specialized hardware based on DSPs, FPGAs, or both, making it difficult to easily port software waveforms (courtesy Altera).

of the transparent interoperability developers are seeking. One reason for this intermediate stage in the SCA's evolution revolves around the fact that the SCA framework primarily targets general-purpose processors, such as the Pentium or the PowerPC. However, to achieve sufficient performance and cost efficiency, most designs today employ specialized hardware based on DSPs, FPGAs, or both (**Figure 2**). The SCA effectively addresses portability for general-purpose processors, but it clearly misses the mark where specialized hardware is concerned. This shortfall is the weakest link in the SCA, because, if you cannot easily port software between platforms, you cannot achieve the required interoperability—or, more accurately, near or sufficient interoperability.

The JTRS is addressing the issue of specialized hardware. A major concern is that designers develop software in a linear and sequential fashion, whereas hardware achieves its highest efficiencies through parallel processing. How a developer defines functions has a major impact on the efficiency of the final implementation. Certainly, it is possible to port a C implementation of a waveform intended to run on a general-purpose processor over to a DSP or FPGA. All you need to do is run the C code through an appropriate tool that converts the function into an FPGA implementation. This step, however, neglects to use the FPGA's primary architectural advantage: extensive parallelism. In fact, the only way to exploit this parallelism is to effectively rework the code, which transforms a simple port into an extensive redesign. At this point, it becomes questionable whether the FPGA actually increases cost.

This problem is difficult to solve. The most efficient code matches the architecture in use: FPGA, DSP, mixed DSP and FPGA, general-purpose processor, and so on. Although requiring software vendors to create such substantially different versions of their code is simply infeasible, a single generic implementation doesn't seem effective either.

The JTRS attempted to address specialized hardware in Version 3.0 of the SCA spec. The hope was to create abstracted processing resources that you could assign to various tasks. Many developers, however, have described the approach as software-oriented and insufficient for capturing DSP and FPGA capabilities. Specifically, the SCA didn't clearly define the level of abstraction, forcing vendors to interpret the spec with the result that each implementation differs sufficiently to be effectively proprietary. Additionally, in some cases, the extra software necessary for implementing the abstraction was enough to completely erode any DSP and FPGA performance advantages. As a consequence, the JTRS has reverted to a previous version of the SCA.

DSPs and FPGAs are essential for creating efficient and cost-effective SCA-based implementations, both in military and commercial applications. General-purpose processors are effective at efficiently implementing generalized tasks but are much less efficient than specialized hardware at implementing well-defined, computationally intensive pro-

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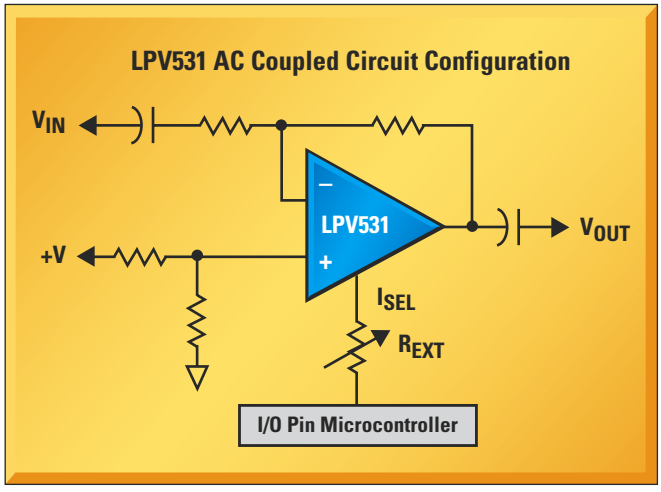

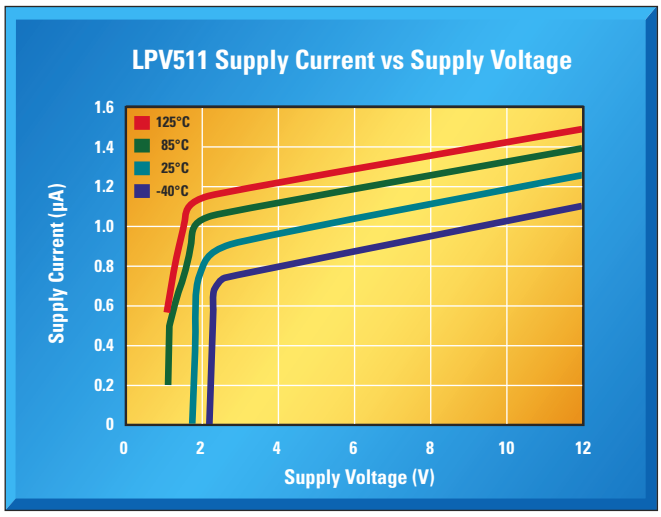

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cessing algorithms, leading to greater power consumption and larger radio form factors—both undesirable results. The JTRS is seeking to leverage the advantages of specialized hardware without tying software to proprietary hardware implementations. After the JTRS was reorganized in 2005, its leadership decided to resolve this issue internally. Although, on the one hand, this approach limits industry participation in shaping the SCA standard, the decision prevents commercial forces from driving changes that will negatively affect how quickly the industry can mandate SCA to military suppliers.

Work is under way to enable the efficient use of specialized hardware in SCA implementations. For example, one of the primary sources of overhead in implementing SCA on an FPGA or DSP is the use of CORBA (Common Object Request Broker Architecture). CORBA is the middleware layer between the operating system and the SCA framework. It transmits data between software objects over a software bus. Implementing CORBA on a DSP or an FPGA is not straightforward. However, several vendors are developing ways to implement CORBA on specialized hardware that would make hardware look more like software without an unreasonable performance compromise.

SDR IN THE INTERIM

Getting SDR to the point at which radios are no longer proprietary platforms is a high priority for the military, and the JTRS continues with its mandate to make this goal possible in the real world, even if some military-radio suppliers are unenthusiastic about the prospect of widening their narrow playing fields to outside competition. SCA is the foundation of this reality.

In the commercial world, however, the SCA framework has a limited hold and perhaps even less appeal. Although many commercial applications could gain an advantage from an SCA-based foundation, the SCA framework perhaps bites off more of the interoperability problem than it can chew. Completely interchangeable hardware and software leads to a market in which the only differentiation is cost. There are few advantages to opening designs in the commercial world simply to invite competition that will drive down profit margins.

The commercial world thrives on innovation, and, in radio applications, hardware is a key differentiator. As it stands, the SCA framework inhibits the introduction of specialized hardware. However, as the SCA standard evolves, there will be much efficiency that you can leverage without adopting the formal standard. In fact, many commercial base stations deployed today have some software-defined basis, given that a significant number of functions, such as remote upload fixes to code, baseband processors that are programmable, and DSPs and FPGAs that can support a variety of waveforms, are software implementations. The base stations use just the bits and pieces, so to speak, that make the most sense.

There is a wide spectrum of adoption for SDR. The military is pursuing the ideal of total interoperability and interchangeability. The commercial world strives to balance efficiency, function, and cost. With such diverse goals and applications, it's almost as if they're dealing with two disparate technologies. EDN

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AUTHOR'S BIOGRAPHY

Contributing Technical Editor Nicholas Cravotta covers digital and communications technologies, including networks, buses, and data security. He is currently developing a unique accessory for the video iPod.

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INTERFACE

Analog Applications Journal

BRIEF

Improved CAN network security with TI's SN65HVD1050 transceiver

By Steve Corrigan • *Systems Engineering, High-Performance Analog Products*

A CAN transceiver must reliably transmit data in extremely harsh operating environments that place an extraordinary electrical burden on the device. Since the transceiver is typically the only interface between expensive node electronics and the CAN bus, many operational security features of the SN65HVD1050 take on additional importance in CAN applications. These features include electromagnetic (EM) immunity, low EM emissions, noise rejection, electrostatic discharge (ESD) protection, fault tolerance, and protection during hot plugging or power cycling.

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EM immunity

As the EM spectrum becomes more fully utilized, due in part to the wireless revolution in electronics, EM interference with other electronic equipment is increasingly becoming a widespread concern.

Every electronic device has its own unique EM characteristics. The inductance and capacitance of any circuit can develop a common-mode resonance at discrete frequencies that either amplify or attenuate emissions.

The HVD1050 CAN transceiver is designed and tested for EM compatibility without malfunction or degradation of performance in rugged EM environments. "Compatibility" in this definition means both low emissions and high immunity to external EM fields.

Low EM emissions: Balanced signaling and common-mode output

An important requirement of products intended for networking applications is that they do not interfere with the operation of other nearby components or systems. The desired behavior is referred to as low-radiated emissions.

EM noise is generated by high-frequency voltage or current switching. In a CAN transceiver, driver output signals are typically mismatched on CANH and CANL, and the resultant EM fields fail to differentially cancel each other as equal and opposite. This output mismatch (displayed in Figures 1 and 2) is referred to in TI datasheets as the peak-to-peak common-mode output voltage, $V_{OC(PP)}$, and can be considered to be a figure of merit for balanced differential signaling.

High immunity: Common-mode noise rejection

Common-mode noise rejection is an inherent feature of true differential receivers. Differential signal pairs are physically

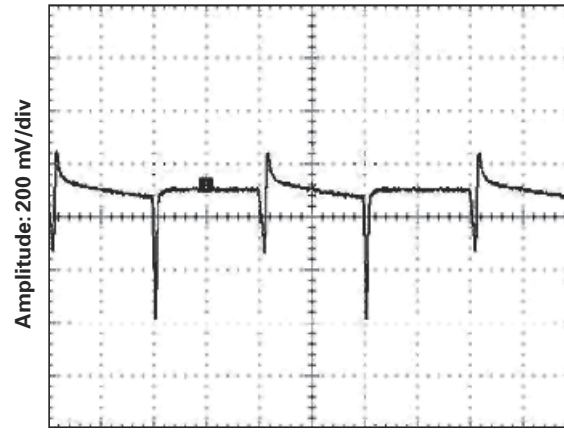

Figure 1. Typical CAN bus $V_{OC(PP)}$ waveform

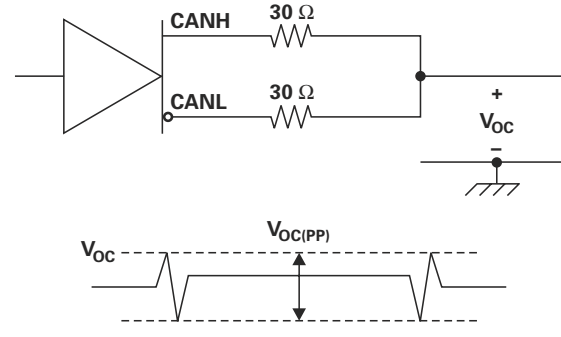

Figure 2. $V_{OC(PP)}$ test setup

close together and have nearly equal exposure to EM sources. This common exposure cancels the influence from magnetic field coupling by reversing the polarity in adjacent loops of twist in twisted-pair wiring.

Unwanted noise of various magnitudes easily links to the antenna-like bus lines of CAN applications. Pulsing motor controllers, switch-mode power supplies, and fluorescent lighting are typical noise sources that couple onto bus lines (displayed in Figure 3).

TI's HVD1050 CAN transceiver is specifically designed and tested for its ability to reject noise over an extremely wide (–12-V to +12-V) common-mode operating range.

Voltage transients and integrated-circuit protection

ESD can occur in any of four ways: A charged body can touch an IC; a charged IC can touch a grounded surface; a charged machine can touch an IC; or an electrostatic field can induce a voltage across a dielectric that is sufficient to break it down. It becomes readily apparent that a high ESD rating indicates not only a robust transceiver but a robust circuit design as well.

The HVD1050 CAN transceiver has an ESD rating of 8 kV when tested in accordance with the Human Body Model (HBM) of JEDEC Standard 22 A114-B, making it much better suited to harsh electrical environments than the earlier transceiver versions of other vendors. To ensure the HVD1050's robustness, it is also tested to ±200 V in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6, and 7.

Fault tolerance

Bus hangs and dominant time-out

CAN bus operators occasionally report that all bus communication comes to a halt when a faulty node places a continuous dominant bit on the bus. This stuck-dominant condition occurs either from a faulty controller or from random slivers of wire, a solder ball, or metal shaving shorts across a transceiver's input (TXD) pin and the adjoining ground (GND) pin.

A dominant time-out circuit in the HVD1050 prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD. If no rising edge occurs before the time-out constant of the circuit expires, the driver is output-disabled, releasing the bus from the stuck-dominant condition. Once the fault is corrected, the circuit is reset by the next rising edge on TXD.

Crushed-cable and short-circuit protection

Bus-cable polarity reversals, accidentally crushed cable, and unintentional shorts of the bus wires to power supplies or ground are common in many CAN applications. The HVD1050 provides short-circuit protection from –27 V up to +40 V. This protection guarantees that the device will continue normal operation once the fault is removed. The HVD1050 also automatically shuts down when thermal conditions exist that could damage internal circuitry.

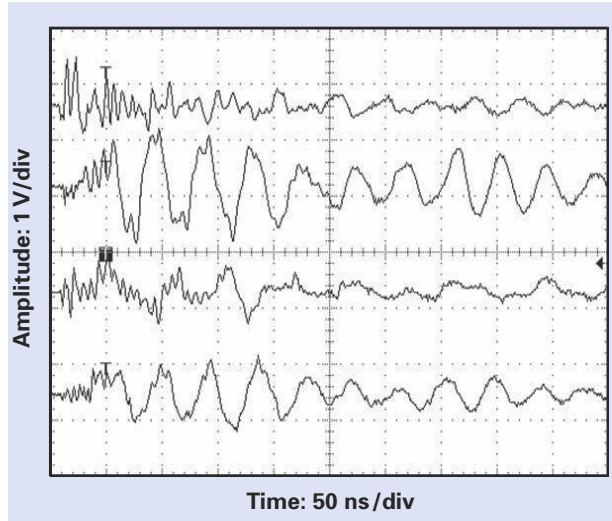

Figure 3. Common-mode noise coupled onto four twisted-pair bus lines

Hot plugging, power cycling, and glitch-free outputs

Adding additional components to a network most often requires shutting down the entire network to prevent costly system errors. Plugging an unpowered module directly into a powered system ("hot plugging") requires that the transceiver output remain stable during the unpowered to power-up transition without disturbing ongoing network communications.

Many CAN transceivers on the market today have a very low output impedance when unpowered. This causes the device to sink any signal present on the bus and effectively shuts down all data transmission. The HVD1050's bus pins are biased internally to a high-impedance recessive state. This provides for a power-up into a known recessive condition without disturbing ongoing bus communication. It also maintains the integrity of the bus when power or ground is added to or removed from the circuit.

Conclusion

CAN applications can place many demands on network interface devices. TI's SN65HVD1050 EMC-optimized CAN transceiver provides cross-wire, over-voltage, and loss-of-ground protection, over-temperature protection, and wide common-mode range. It withstands significant voltage transients. The ruggedness and up to 1-Mbps signaling rate make the HVD1050 ideal for many industrial and automotive applications.

References:

1. App Note SLOA101, Introduction to the Controller Area Network
2. App Note SLOS346H, 3.3-V SN65HVD230 CAN Transceiver Family
3. App Note SLLS557D, 3.3-V SN65HVD233 CAN Transceiver Family

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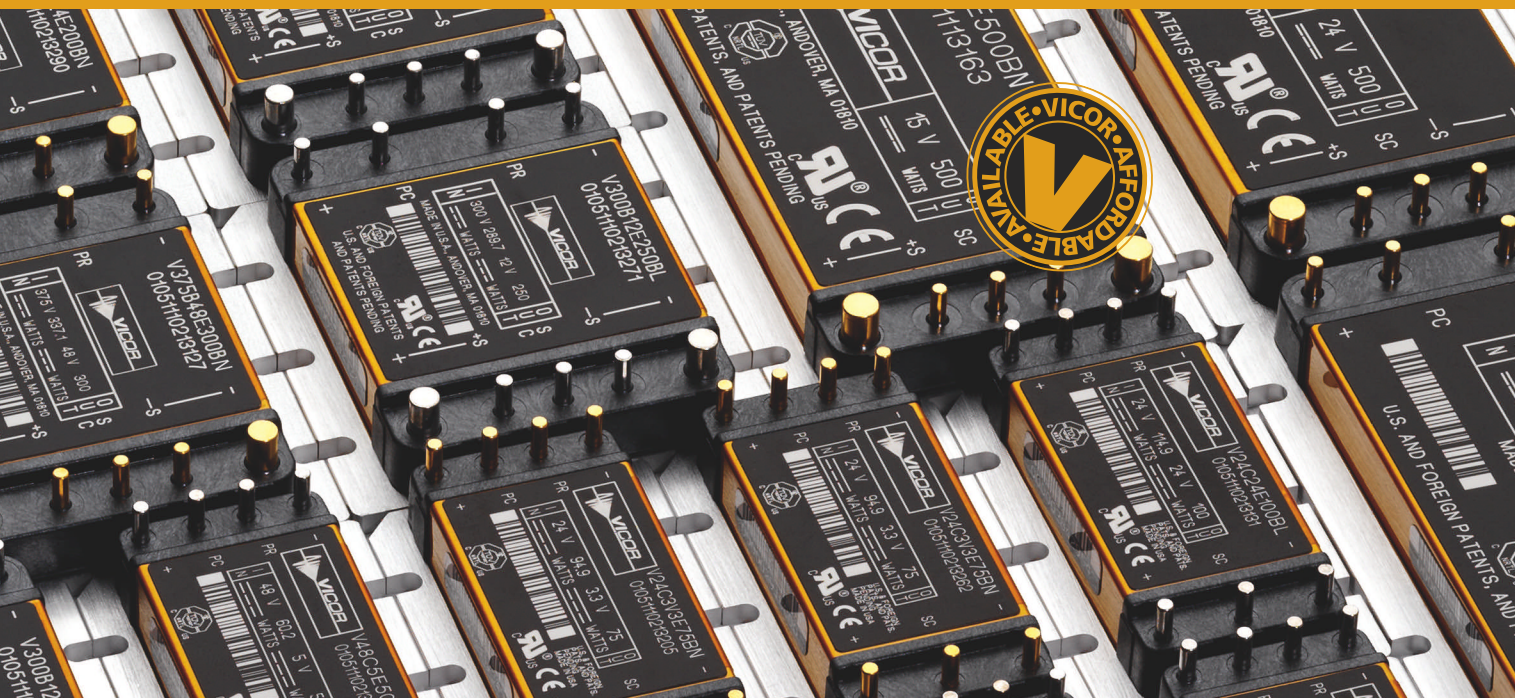
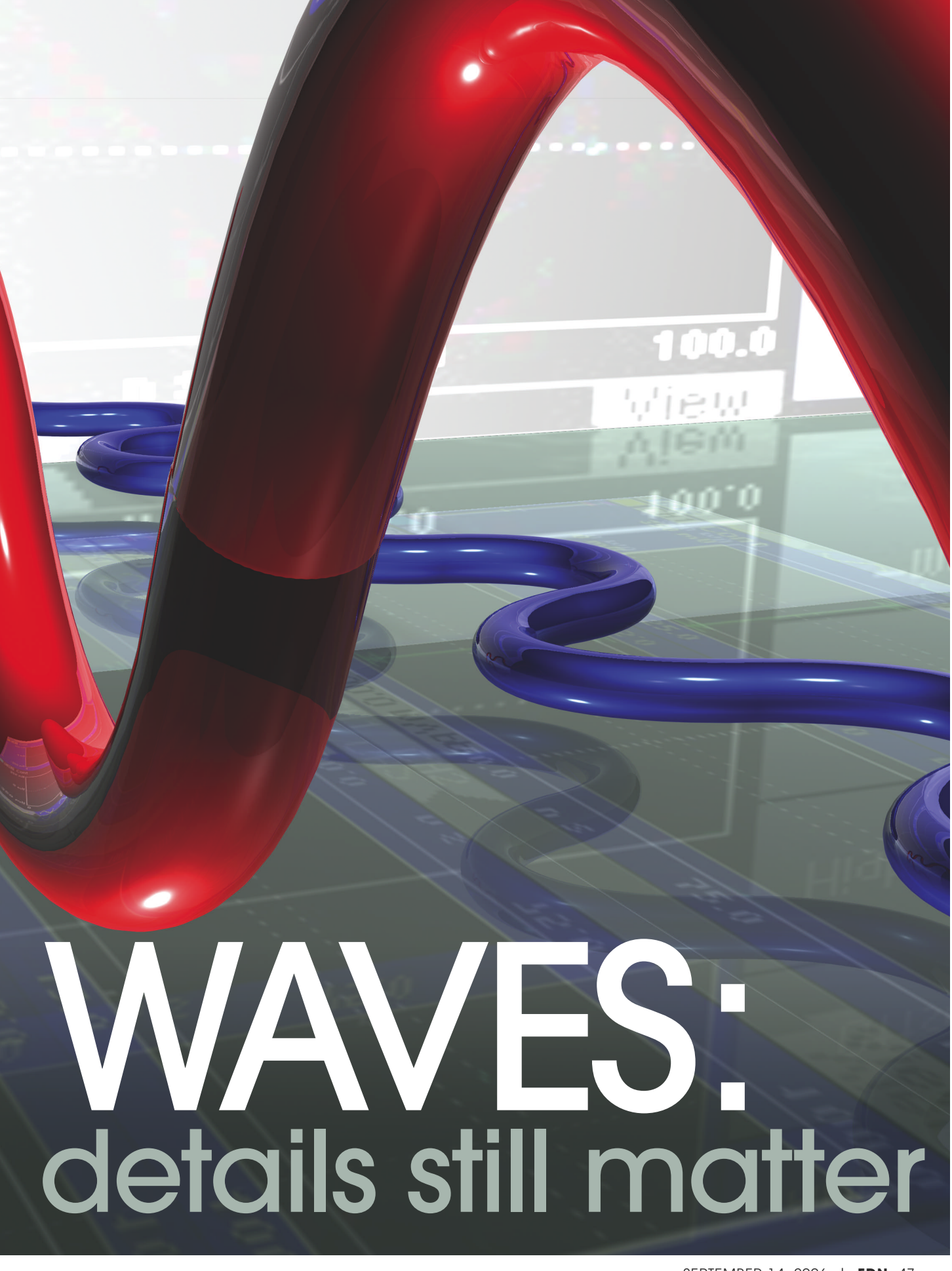


It would be untrue and grossly unfair to the test-and-measurement industry to say that, in the eight years since *EDN* published an article on waveform generators (**Reference 1**), the technology and the products have remained unchanged. The most obvious change is the disappearance of some of the manufacturers mentioned in '98—although those companies' product lines are mostly still available from the companies that acquired the businesses. Strikingly, though, despite the appearance of many improvements and higher performance products and the fact that a 2006 dollar buys more waveform-generation capability than did a 1998 dollar, the underlying technology has remained surprisingly stable. Except for some new features, the block diagrams of most 2006 waveform generators are remarkably similar to those of 1998 instruments. Moreover, the need to understand the specifications and operation of the waveform-generation products that you buy today is just as important as was that need eight years ago.

BY DAN STRASSBERG • CONTRIBUTING TECHNICAL EDITOR

UNDERSTANDING WAVEFORM-GENERATOR OPERATION AND SPECIFICATIONS BEFORE YOU BUY IS AS IMPORTANT TODAY AS IT WAS EIGHT YEARS AGO.

MAKING Eight years later,



WAVES: details still matter

AT A GLANCE

Selecting a waveform generator can be confusing. Vendors use different terminology to describe their instruments' architecture. You need to carefully study the data sheet to determine an instrument's important characteristics. Failure to do so is likely to result in unpleasant surprises.

Generators that use DDS (direct-digital synthesis) provide impressive features at attractive prices, but there are two basic ways to build DDS-based generators of user-defined arbitrary waveforms. For such waveforms, DDS-based true AWGs (arbitrary-waveform generators) are more flexible and generally more expensive than SFGs (synthesized-function generators).

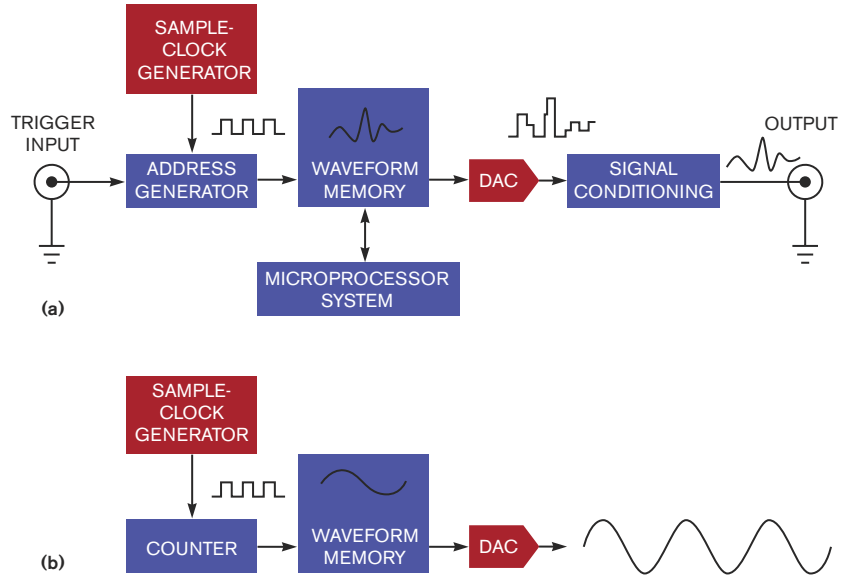


Figure 1 Whereas the block diagram of a true arbitrary-waveform generator (a) and that of an SFG (synthesized-function generator) are similar, the SFG usually lacks the microprocessor system and uses relatively simple filters in the signal-conditioning block. In a generator of fixed functions (b), the sample-clock generator may be DDS-based (courtesy Wavetek).

Even though their underlying technology is digital, the waveform generators that this article covers all produce analog waveforms. Generators that are analog throughout are still being manufactured—just as are analog oscilloscopes, but, like analog scopes, analog waveform generators are now restricted almost entirely to low-cost units whose primary market is in education. Internally digital generators range from units that produce sinusoidal signals whose output frequencies max out at a few megahertz to units that can deliver sine waves at frequencies as high as 500 MHz. Upper frequency limits for sinusoidal outputs are more commonly only 50 or 80 MHz, however. When producing nonsinusoidal waveforms other than square waves, these generators' maximum output frequencies are usually lower, although the maximum square-wave frequency is often equal to the maximum sine-wave frequency.

Prices for high-quality waveform generators begin at a little more than $1000 and range upward to more than $50,000

TABLE 1 WAVEFORM-GENERATOR ARCHITECTURES

Parameter	DDS-based synthesized-function generator	Arbitrary-waveform generator (ARB, AWG)	Tabor Wonder Wave series*
Sampling rate	Fixed	Variable	Variable to 1.2G samples/sec
Waveform type	Standard plus limited arbitrary	Arbitrary	All standard, arbitrary, and captured waveforms
Vertical resolution	Typically 14 bits	To 16 bits	To 16 bits
Memory depth	To 14k points	To 4M points	To 16M points
Memory management (sequencer)	No	Yes	Yes, as many as 16,000 segments, four advance modes
Signal integrity	Can skip or add points	Precise	Precise
Jitter and phase noise	High	Low	Low
Modulation	All frequency modulation	Amplitude modulation or none	All frequency, amplitude, and phase modulation, including digital
Frequency sweep	Yes	Limited	Yes
Trigger modes	Some	Yes	Continuous, trigger, burst, gated, retrigger
Amplitude range	10V p-p into 50Ω maximum	10V p-p into 50Ω maximum	To 32V p-p into open circuit
Digital outputs	No	Some	Yes
Ability to synchronize multiple instruments	No	Yes	Yes with extended facilities
Cost	Affordable	Can be expensive	Affordable

*True AWG with DDS clock and additional proprietary features (courtesy Tabor)

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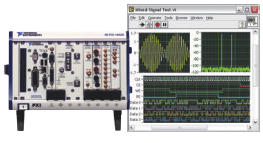

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Digital Multimeters	Up to 7½ digits, LCR, 1,000 V
Programmable Power Supplies	Up to 20 W, 16 bits
Audio Analyzers	Up to 24 bits, 500 kS/s
Switches	Multiplexers, matrices, RF, relays
Multifunction I/O	Analog I/O, digital I/O, counters

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for the highest performance units. The generators this article discusses—even the ultrawide-bandwidth units that can produce signals at hundreds of megahertz—are usually thought of as baseband devices. Nevertheless, most generators that produce signals at frequencies beyond 80 MHz are categorized as RF-signal sources. Unlike baseband generators, however, RF generators can usually produce both modulated and unmodulated carriers. In most cases, RF generators include modulation sources. But these instruments usually also accept modulation signals from external sources, such as the baseband generators discussed here. Often—especially when the modulation is digital—the baseband generator must produce two independent outputs, I (in-phase) and Q (quadrature), because many forms of digital modulation depend on separately controlling the RF signal's I and Q components (see **sidebar** "Using waveform generators in IQ-modulator characterization" at the Web version of this article at www.edn.com/060914cs).

Several architectures dominate waveform generation (**Figure 1**). Probably the most common, albeit not the most familiar, is the SFG (synthesized-function generator), or function synthesizer. The SFG architecture is a clever elaboration on DDS (direct-digital (frequency) synthesis). The more familiar architecture is that of the ARB or AWG (arbitrary-waveform generator). In all likelihood, the reason that the ARB architecture is more familiar is that designers more easily understand it at the block-diagram level—though not necessarily at the detailed implementation level. Some generators—even relatively inexpensive ones—employ both architectures, using each architecture to perform those functions the instrument designers believe it performs best.

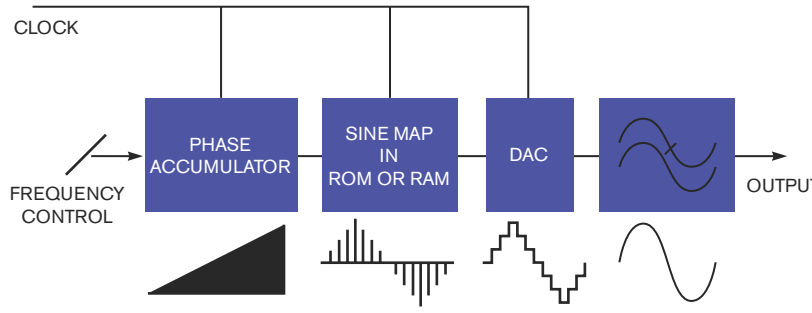

Figure 2 SFGs and most AWGs that have swept-frequency capabilities use clock generators based on the DDS technique known as phase accumulation.

According to the company, Tabor's Wonder Wave series (**Table 1**) delivers, without compromise, the best features of AWGs and SFGs at prices approaching those of SFGs, which are generally less expensive than AWGs. Although this impressive claim suggests an architectural breakthrough, the generators are true AWGs that use DDS-based clocks.

STRENGTHS, WEAKNESSES

It is important to understand the strengths and weaknesses of the architectures and how these characteristics can either suit a generator for a certain job or provide a reason for you to select a different model for your application (**Table 2**). A lack of understanding can lead you to discover too late unexpected performance quirks that make using the generator considerably more difficult than you expected.

One complication in evaluating waveform generators is that manufacturers are

TABLE 2 GUIDE TO SELECTING WAVEFORM GENERATORS BY APPLICATION

	Generator category			
Criteria	**Function/ sweep**	**Arbitrary/ function (SFG)**	**Arbitrary waveform**	**Vector signal**
Frequency				
To 20 MHz	X	X		
20 to 240 MHz		X	X	
Greater than 240 MHz			X	X
Waveform characteristics				
Standard (sine, square, triange, sawtooth, ramp, noise, etc)	X	X		
Long, complex, fast transitions			X	X
IQ-modulation signals		X	X	X
Application				
High-speed serial data (PCI Express, SATA, HDMI)			X	
Low-speed serial data (I^2C, CAN, and others)		X		
RF test (wireless communication, RF, baseband, UWB, defense)		X	X	X
Optical- and magnetic-storage testing			X	
Digital test (mixed-device components, DAC, ADC, memory)			X	
Image-device test (capture and display)		X	X	
Other (automotive, education, medical)	X	X	X	
Available budget				
To $1500	X			
$1500 to $10,000		X		
More than $10,000			X	X

(Table courtesy Tektronix)

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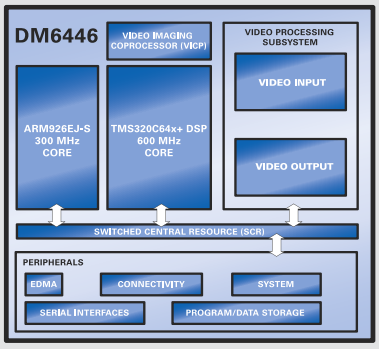

Performance Benchmarks:

STANDALONE CODECS	DM6446	DM6443
MPEG-2 MP ML Decode	1080i+ (60 fields /30 frames)	720p+
MPEG-2 MP ML Encode	D1+	n/a
MPEG-4 SP Decode	720p+	720p+
MPEG-4 SP Encode	720p+	n/a
VC1/WMV 9 Decode	720p+	720p+
VC1/WMV 9 Encode	D1+	n/a
H.264 (Baseline) Decode	D1+	D1+
H.264 (Baseline) Encode	D1+	n/a
H.264 (Main Profile) Decode	D1+	D1+

+ denotes available processor headroom for analytics and/or other features

Tools: Validated Software and Hardware Development

- DVEVM (Digital Video Evaluation Module)
- MontaVista Development Tools
- Code Composer Studio IDE

Software: Open, Optimized and Production Tested

- Platform Support Package
- MontaVista Linux Support Package
- Industry-recognized APIs
- Multimedia frameworks
- Platform-optimized, multimedia codecs:
  - H.264
  - MPEG4
  - H.263
  - MPEG2
  - JPEG
  - AAC+
  - AAC
  - WMA9
  - MP3
  - G.711
  - G.728
  - G.723.1
  - G.729ab
  - WMV9/ VC1

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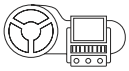
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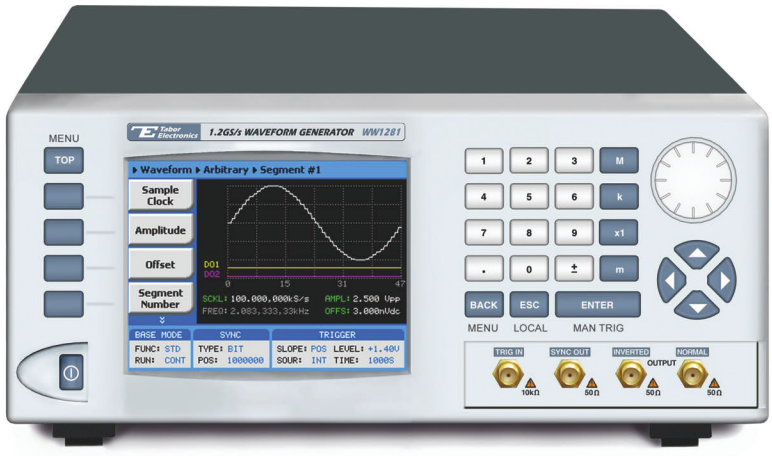
often inconsistent in their use of such terms as ARB. Many SFGs, though best at generating standardized waveforms, such as sine, square, sawtooth, and triangular waves, can, within limits, produce arbitrary waveforms. Adding such capabilities to an SFG does not add tremendous cost, and users who believe that they may someday need to generate arbitrary waveforms find the feature an attractive security blanket. Unfortunately, the manufacturers sometimes describe these SFGs as ARBs or AWGs, even though the instruments can't match the arbitrary-waveform-generation capabilities of generally more expensive, true ARBs. Some manufacturers use the term "AFG" (arbitrary-function generator) to denote instruments that are basically SFGs but also offer limited arbitrary-waveform-generation capabilities.

Further complicating product selection is the fact that many true ARBs use DDS to generate their swept-frequency clocks (**Figure 2**). Whereas DDS is well-suited to generating frequency sweeps and a sweep capability is an important attribute of most SFGs, not all AWGs that use DDS to produce swept-frequency clocks deliver the best combination of AWG and SFG attributes.



Tabor's WW1281 boasts 400-MHz bandwidth and true-AWG capabilities, including deep memory. The manufacturer claims that the generator family offers all of the advantages and none of the drawbacks of SFGs and true AWGs at prices close to those of SFGs.

THE PHASE ACCUMULATOR

The heart of an SFG is the phase accumulator. This elegant functional block converts a reference clock at a fixed-frequency, f_C, into a stable, lower frequency output clock whose frequency, f_O, you can set with great precision over a wide range and change essentially instantaneously in tiny, huge, or in-between steps. In addition, the output signal's phase is continuous when the frequency changes. That is, if you command the frequency to change from, say, 10 MHz to 100 kHz at the 227° point of an output cycle, the 100-kHz waveform begins at its 227° point. Moreover, if the phase accumulator drives a DAC that produces an analog output, no discontinuity occurs in the output amplitude—only a change in slope if the output is a sine wave or another continuous waveform.

DDS is well-suited to producing swept frequencies because you command the phase accumulator to produce a particular value of f_O by supplying it with a binary number, M. (Implementations also exist in which M is in binary-coded-decimal format.) The greater the value of M, the higher the output frequency. If you continuously vary M, f_O continuously varies. By supplying values of M that change over time in appropriate ways, you can create a limitless variety of sweep types, of which linear and logarithmic ramps, sawteeth, and sinusoidally varying frequencies are probably the most common.

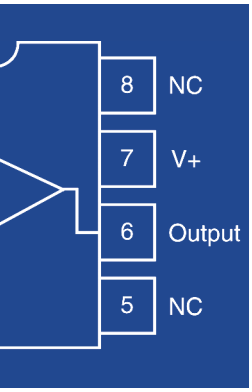
You can think of this approach as dividing an output cycle into 2^N intervals or steps. Suppose N=14; then, 2^N=16,384 and each step represents 360°/16,384 or 0.02197°. If N=14 and M=2048, the sample points occur at 45° intervals, and $f_O=f_C/8$. If M=1, the sample points occur at 0.02197° intervals and $f_O=2^{-14}\times f_C$. In this example, the values of M are powers of 2, but in a real system in which N=14 (actually a somewhat simplified version of a real system), M would be a 14-bit binary number and could therefore assume any integer value from 1 to 16,384. An output cycle need not contain an exact integer number of sample periods, however. Indeed, the lack of such a requirement makes possible the synthesizer's superb frequency resolution—that is, its ability to let you adjust f_O in such tiny increments.

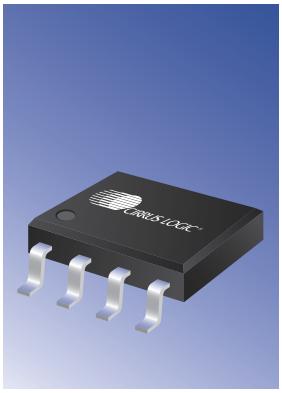
This digital-frequency synthesizer is a sampled-data system and is subject to the limitations of the sampling theorem. In the preceding example, the theoretical maximum output frequency is incrementally less than $0.5\times f_C$. The practical maximum is somewhat lower—approximately $0.4\times f_C$.

BK Precision's DDS-based, 21-MHz-bandwidth 4070A offers many attractive features at a moderate price.

OTHER FUNCTIONAL BLOCKS

Although the phase accumulator is a key element in an SFG, it isn't the whole instrument. To produce analog waveforms, the instrument must convert the frequency synthesizer's swept- or variable-frequency output into an analog waveform. This conversion requires a waveform memory, a DAC, and output-signal conditioning—which often includes deglitching of the DAC output, always includes filtering, and usually includes amplification. With the frequent exception of square waves, which designers usually think of as trivial, the data sets that define the standard waveforms reside in





Applications

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- Foundry Process Automation
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The CS3003/3004 family of ICs offer open-loop gain of up to 150 dB (typical) and input offset voltage of only five microvolts, with drift of 0.05 microvolts per degree. Critical noise errors are limited to 17 nanovolts per root-hertz, which is held flat above 2 kHz bandwidth. This exceptional performance ensures minimal errors due to noise, leakage and drift while offering extremely high gain to preserve measurement accuracy.

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With these new products, Cirrus Logic has strengthened its portfolio of high-precision analog ICs for applications demanding superior high-resolution measurement.

ROM look-up tables. Sometimes, even the square-wave data sets reside in ROM, as this approach permits precise control of rising- and falling-edge slew rates. For user-defined—that is, arbitrary—waveforms, the look-up tables reside in RAM instead of ROM. As f_O increases, the number of points in the waveform definition decreases. In other words, as f_O increases, the generator skips sending more and more of the values from the look-up table to the DAC. Conversely, at low values of f_O, the generator may repeatedly send some or all of the values from the look-up table to the DAC before moving to the next value in the data set.

Although it is not intuitively obvious, an SFG that uses a single-frequency clock to provide the input to its frequency synthesizer, as do most SFGs, does not need output lowpass filters whose corner frequency depends on the output signal's repetition rate. The ability to use relatively simple fixed-frequency output filters is a key reason that SFGs can be highly cost-effective.

Though they offer a large number of highly desirable characteristics, SFGs are, nevertheless, not perfect. For example, the fact that a generator may skip points in the waveform-definition look-up table at high values of f_O and may repeat points at low values of f_O suggests that the output waveforms are not completely predictable. Moreover, because M, the number that determines f_O, need not be an integer submultiple of the look-up-table depth, cycle-to-cycle variations can easily occur in the waveforms. That is, on successive iterations of the output waveform, different look-up-table points will repeat or be absent. Thus, SFG outputs, though extremely stable in average frequency over the long term, can exhibit troublesome cycle-to-cycle variations in the short term. You can correctly characterize these variations as jitter.

For builders of test systems, several companies offer waveform generators as modular instruments. LeCroy's PXI-based PXA125 re-creates data sets as deep as 2M points at 125M samples/sec.

In addition, whereas waveform-memory depths of 2^{14} (16,384) points—the value in several popular SFGs—may sound generous, user-defined waveforms are often as much as 16M points deep. Moreover, users may want to effectively modify the waveform depth on the fly by repeating waveform segments, often through the use of conditional branching and looping. In the waveform-generator context, conditional branching is the ability to jump to a specified point in the waveform-definition table after satisfying a test condition. Looping is the ability to repeat a range of waveform-definition points either a specified

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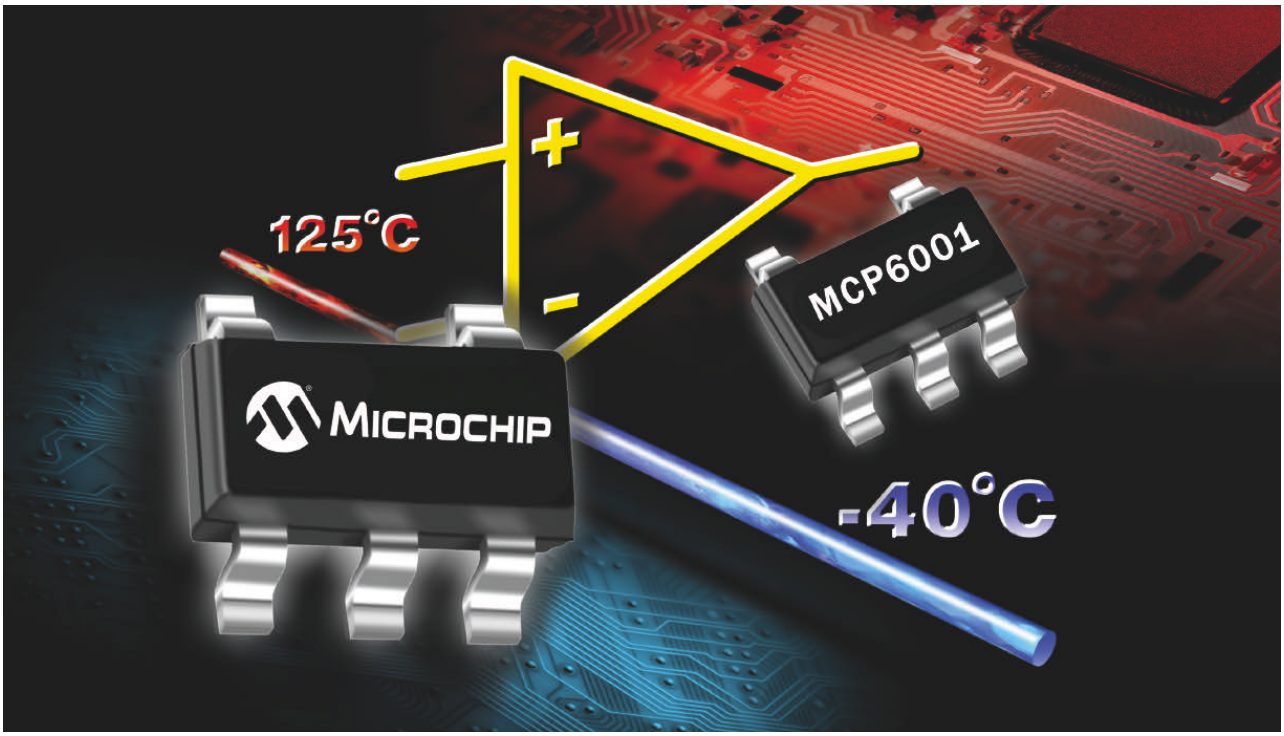

Select Standard Op Amps

Part #	GBWP	Iq Typical (µA)	Vos Max (mV)	Input Voltage Noise Density @ 1 kHz (nV/√Hz)	Operating Voltage (V)
MCP6041/2/3/4	14 kHz	0.6	3.0	170	1.4 – 5.5
MCP6141/2/3/4	100 kHz	0.6	3.0	170	1.4 – 5.5
MCP6231/2/4	300 kHz	20	5.0	52	1.8 – 5.5
MCP6241/2/4	550 kHz	50	5.0	45	1.8 – 5.5
MCP6001/2/4	1 MHz	140	4.5	28	1.8 – 5.5
MCP6271/2/3/4/5	2 MHz	170	3.0	20	2.0 – 5.5
MCP6281/2/3/4/5	5 MHz	445	3.0	16	2.2 – 5.5
MCP6291/2/3/4/5	10 MHz	1100	3.0	8.7*	2.4 – 5.5
MCP6021/2/3/4	10 MHz	1000	0.5	8.7*	2.5 – 5.5

* Value is typical at 10 kHz

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number of times or until some test condition is satisfied. Although such capabilities are common in ARBs, no SFG currently on the market offers these features, and it is unclear that such capabilities would be consistent with the SFG architecture.

AWGs: SIMPLE IN CONCEPT

It would be convenient to say that AWGs developed as a result of SFGs' shortcomings, but AWGs predate SFGs and have evolved into the dominant high-end waveform-generation products as SFGs captured an increasing share of the high-volume applications. Conceptually, AWGs are simple: A clock, which can use DDS, drives a counter, which supplies addresses to the waveform memory. For arbitrary waveforms, the memory is always RAM. The sequencing logic, which makes possible the looping and branching capabilities, stands between the counter output and the memory-address lines. The data-set values from the memory become the input to a DAC, which drives analog-signal-conditioning circuits that supply the output signal. From a block-diagram perspective, the AWG's signal conditioning is much the same as that of the SFG, although, in practice, the filters can differ significantly.

Strictly speaking, although you can use a DAC on a PC-plug-in data-acquisition board to generate arbitrary waveforms, such a board does not fit the definition of an AWG. For example, data-acquisition boards incorporate no looping-and-branching memory-addressing logic. And, whereas a data-acquisition board may provide a means of adjusting the DAC's offset and full-scale-output voltages over narrow ranges, if you want to reduce the full-scale output from, say, 10.24 to 5.12V, either you must furnish your own output attenuator, thereby increasing the output-source resistance, or you must divide the DAC's digital inputs by two, thereby reducing the unit's resolution. On the other hand, many instrument-level AWGs have wide-range gain controls that require neither of these compromises.

Although data-acquisition boards aren't AWGs or SFGs, true AWGs and SFGs are available not only in familiar benchtop-instrument formats, but also as modules in such formats as CompactPCI and PXI, as well as in standard PC-plug-in—that is, PCI—formats. Among the suppliers are LeCroy, National Instruments, and VXI Technology.

Fluke's 291 is part of a series of one-, two-, and four-channel DDS-based generators that reproduce data at speeds to 100M samples/sec. Despite the high speed, the unit's price is close to those of some generators with much lower performance.

Output filtering is an area in which AWGs and SFGs can differ significantly. As stated, SFGs work well with relatively simple fixed-frequency lowpass filters. In contrast, AWGs can sometimes benefit from output lowpass filters whose −3-dB frequency, $f_{-3\,dB}$, is a constant fraction of the clock frequency. With a DDS-based clock, $f_{-3\,dB}$ would thus be a constant fraction of the DDS-output frequency. The problems with this approach, however, are its complexity and cost. As a result, practical generators sometimes settle for a few switchable, fixed-frequency filters.

In an AWG, there is merit to making $f_{-3\,dB}$ and perhaps the shape of the filter's stopband response user-selectable and not linking $f_{-3\,dB}$ to the clock frequency. The generator's designer has, at best, only a vague idea of the complexity of the waveforms the instrument users will want to synthesize. At a given repetition rate, more complex waveforms have greater high-frequency content than do simpler ones and may require a more complex filter topology, a higher $f_{-3\,dB}$, or both. Using DSP to shape the values of the data-set points that define the waveform before applying the values to the DAC might be a way to optimize the generator's frequency response and minimize the filter requirements. The multimedia world uses upsampling, in which DSP techniques fill in intermediate values

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in sparsely sampled, bandwidth-limited data sets, thus simplifying the reconstruction of analog signals from sampled data. Such techniques might also work in waveform generators. Nevertheless, no commercial baseband waveform generator currently uses either approach.

DON'T GET CARRIED AWAY

Companies that market waveform generators emphasize that the biggest problems their customers experience with the products involve learning to use the more arcane features, especially defining arbitrary waveforms. Although many generators that produce arbitrary waveforms require a separate computer running appropriate software for creation of waveform-definition files, some generators include built-in waveform-definition applications. Users who lack experience with these applications and who believe that they can learn by creating a complex waveform that they need *now* are likely to suffer disappointment and frustration. Even for experienced users of waveform-definition applications, the creation of complex waveforms takes time. You should gain facility with such applications by first learning how to define relatively simple waveforms, and, to do so, you should set aside adequate learning time when you are not under pressure. You should try defining complex signals only after you have mastered the basic operations, and, again, you should avoid working on complex definitions when you are under time pressure.

Generally speaking, waveform-generator user interfaces are only moderately complex. Many newer instruments have front-panel waveform displays that give the generators the look of oscilloscopes. To the uninitiated, this appearance can be deceiving. Few of these instruments provide displays of actual output waveforms. Rather, the displays give you an idea of such waveform characteristics as rise time when you are specifying them.

Although the number of bits of vertical resolution in waveform-definition data sets is important, don't assume that a generator's vertical accuracy necessarily equals the full-scale output divided by 2^N, where N is the number of bits. Look instead for a specification of vertical resolution as a percentage of full scale; it is likely to correspond to a slightly smaller effective number of bits because of static and dynamic errors in the DAC and signal-conditioning circuits. Remember, too, that both the actual and the effective word length tend to be lower in generators with higher bandwidth. If you can find an instrument that simultaneously delivers 16 effective bits of resolution and 500-MHz bandwidth, it is likely to cost you dearly. EDN

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AUTHOR'S BIOGRAPHY

Contributing Technical Editor Dan Strassberg has covered test and measurement for EDN *for nearly 19 years. He holds two degrees in electrical engineering—a bachelor's from Rensselaer Polytechnic Institute (Troy, NY) and a master's from the Massachusetts Institute of Technology (Cambridge).*

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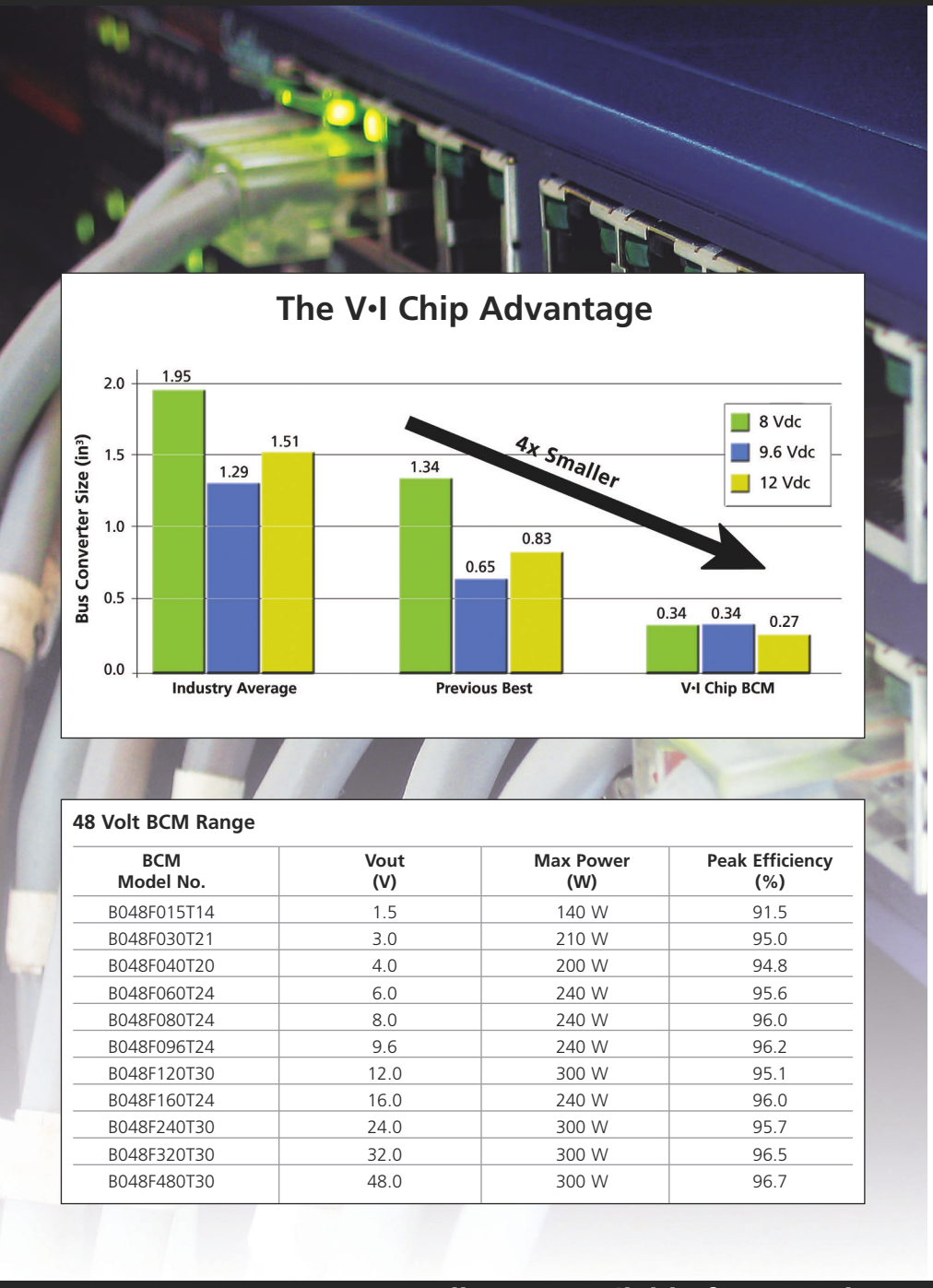

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B048F080T24	8.0	240 W	96.0
B048F096T24	9.6	240 W	96.2
B048F120T30	12.0	300 W	95.1
B048F160T24	16.0	240 W	96.0
B048F240T30	24.0	300 W	95.7
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ADVANCED SIGNAL-CONDITIONING TECHNIQUES CAN SOLVE INTERCONNECT PROBLEMS.

Designing system interconnect isn't the most glamorous engineering job in the world. Indeed, to most system or digital designers, being assigned a backplane, interconnect, and connector selection is tantamount to being told to go stand in a corner with a pointy hat. In reality, what they need is a wand with that hat, because a lot of magic has to happen to make problems disappear.

Designers and system architects are realizing that the number of interconnections between functional blocks in systems is becoming unwieldy. Indeed, Moore's Law not only applies to the number of transistors that you can pack onto an IC, but also drives the amount of data to transfer between chips, modules, and systems. Classically, the digital information coding this data simply scales by increasing the number of parallel signals. This scaling continues until N interconnects multiply the bandwidth, which the maximum clock speed in the system dictates. The tricky part for the designer was to maintain phase alignment across N signal lines to a single clock line. A few years ago, clock speeds increased to the point at which phase alignment between bits and their clock was marginally operational, driving even wider system buses to accommodate information-transfer needs.

THE BANDWIDTH SHELL GAME

The PC industry, which silicon suppliers primarily drive, has recognized the ugly trend of I/O-count proliferation and recently sounded a death knell for parallel interfaces—first by eliminating the parallel interfaces to peripherals, such as DVD and hard disks, with SATA (serial ATA) and then by defining a serial peripheral interface such as PCI Express. SATA operates at a native rate of 1.5 and 3 Gbps and will soon deliver 6 Gbps; PCI Express delivers 2.5 Gbps per lane (available with one, four, and eight serial lanes), soon scaling to 5 Gbps per lane. The architects of these serial interfaces cleverly disguised them to make the interface indistinguishable to software, above the transport layer, from their legacy parallel implementations.

Chip manufacturers aren't the only ones reaping the benefits of serial interfaces. These interfaces reduce the number of pc-board and cable interconnects by as much as two orders of magnitude. But they may still deliver an increase in informa-

TABLE 1 SERIAL PROTOCOLS AND RATES

Protocol	Data rate (Gbps/lane)
PCI Express 1.1, 2.0	2.5, 5
OIF CEI 6G	6.25
Gigabit Ethernet	1.25, 2.5
Serial Rapid I/O	1.25, 2.5, 3.125
XAUI	3.125, 3.7
SDI	0.270, 1.488, 2.97
SONET	0.62208
Fibre Channel	1.063, 2.125, 4.25

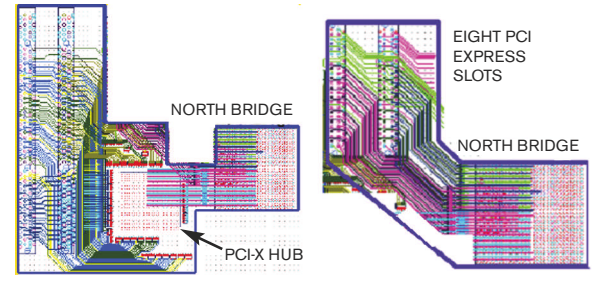


Figure 1 This PCI Express interface delivers twice the bandwidth in half the number of interconnects (courtesy Mentor Graphics).

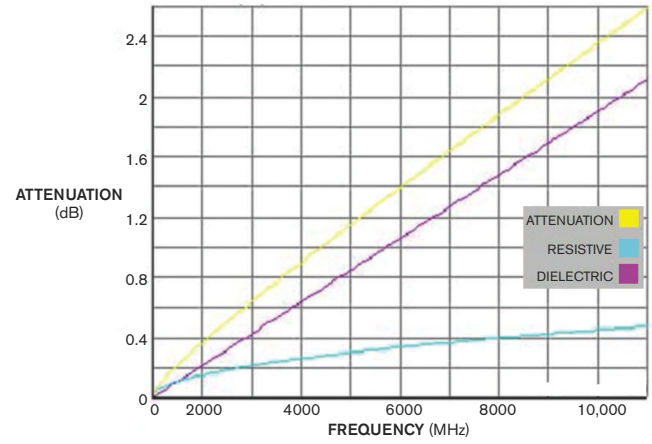
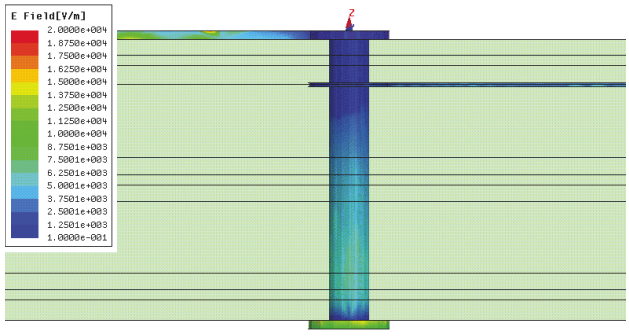
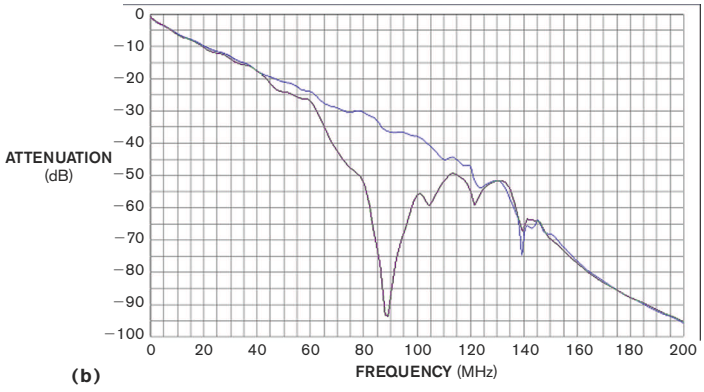


Figure 2 The dielectric-loss component dominates resistive loss for interconnect attenuation above 500 MHz for a representative trace geometry and materials set (courtesy Mentor Graphics).



(a)



(b)

Figure 3 A barrel of metal lacking an end-to-end electrical connection can resonate with strong electromagnetic fields (a, courtesy Leonard Dieguez). The response of a 1.25m counterbored FR408 Molex backplane with GbX connectors reveals that low frequencies are moderately attenuated, but there is also a linearly increasing attenuation of the signal with frequency (b, courtesy Mentor Graphics).

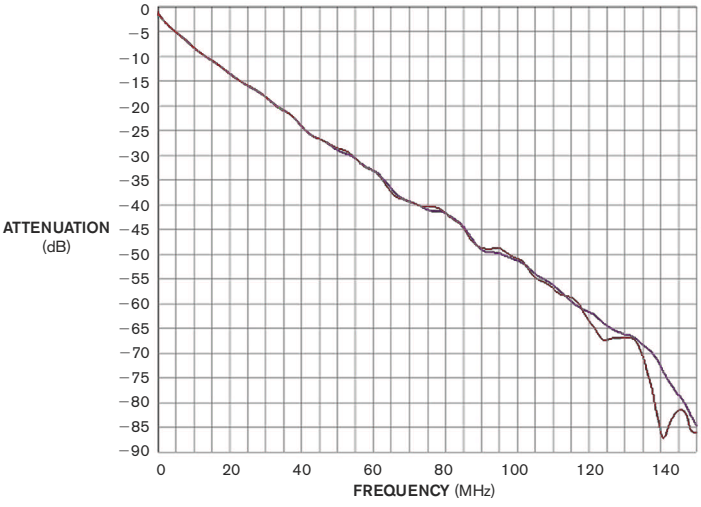
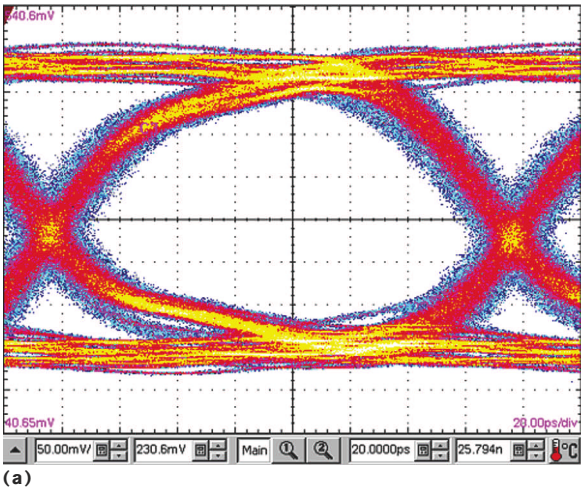
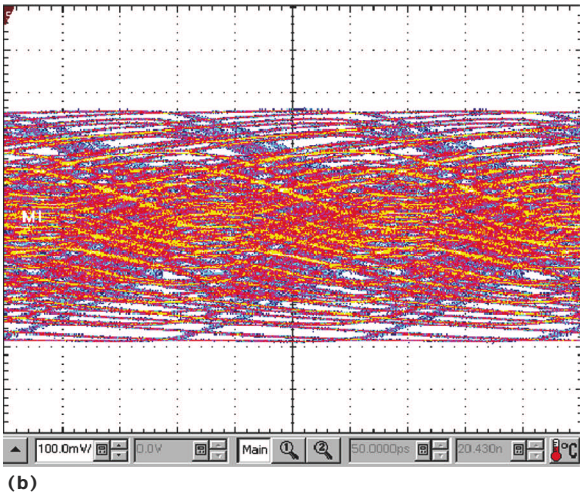


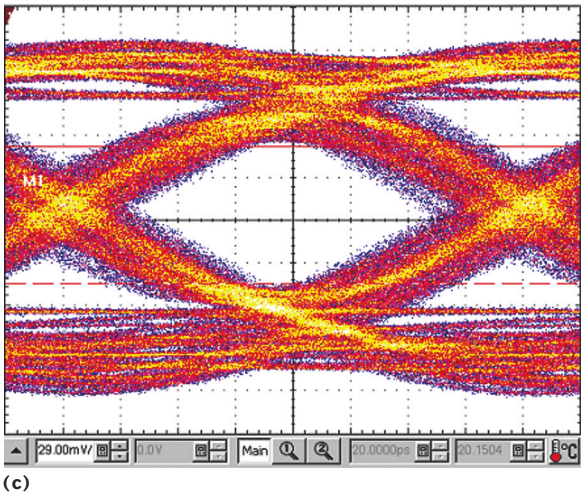
Figure 4 Modeling and actual measurements show excellent correlation for a back-drilled Molex backplane (courtesy Mentor Graphics).



(a)



(b)



(c)

Figure 5 Waveforms depict an FPGA transmitter PRBS eye at 6.25 Gbps with no pre-emphasis (a), a received backplane PRBS eye at 6.25 Gbps after 1.25m (b), and a received backplane PRBS eye at 6.25 Gbps after 1.25m and pre-emphasis from an FPGA (c).

THE 1-Wire ADVANTAGE

Solve System Identification, Authentication, and Product-Protection Problems

1-Wire® devices lower system cost and simplify design with an interface protocol that supplies control, signaling, and power over a single-wire connection.

Problem #1—PC-Board ID and System Configuration/Monitoring

Does your system require

- A unique electronic serial number for system/board identification?
- A simple way to store PC-board configuration, calibration, or manufacturing data?
- A means to identify the physical location of a board in a rack system or multicard environment and to monitor environment conditions?

Solution

- Factory-programmed, unique 64-bit ROM serial numbers in all 1-Wire devices
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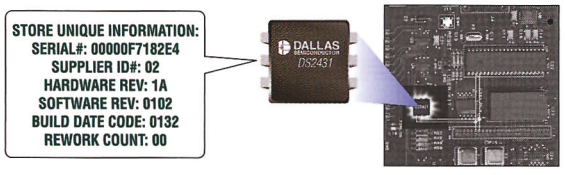
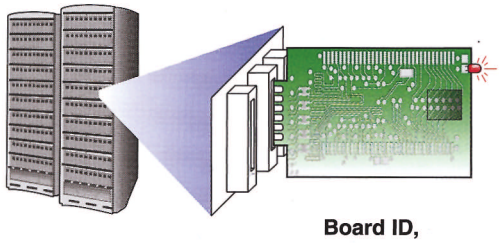


PC-Board ID



Board ID, Location, Control

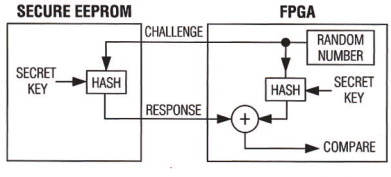
Problem #2—Protect IP and Designs from Unauthorized Cloning

Does your system require

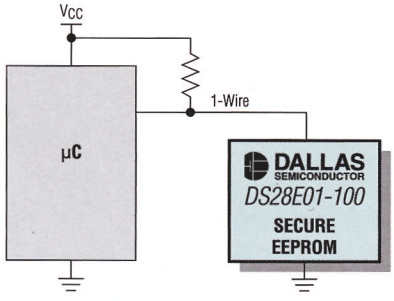
- Safeguards against unauthorized copying of a reference design?
- Secure memory to control system feature settings?
- Protection against altering or copying of FPGA data, system firmware, and other valuable or confidential system data?

Solution

- Low-cost 1-Wire memory devices offer a variety of security levels, including world-class challenge-and-response mutual authentication based on the SHA-1 algorithm (FIPS 180-1,2; ISO/IEC 1011-3)



IP Protection (e.g., FPGA Bitstream)



Secure Feature Setting or µC Firmware Protection

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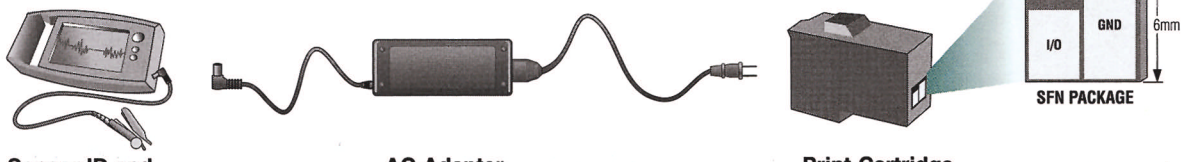
Problem #3—Control and Identify Accessories, Sensors, and Peripherals while Protecting Against Inferior Substitutes

Does your system contain

- Accessories or plug-ins that the host system must identify or control, perhaps after first being properly authenticated to the system?
- A connector or other interface where the number of connection points is constrained, yet data or control information must pass between the host and the peripheral?
- Accessories or peripherals that might be subjected to high ESD levels when being handled by the user?

Solution

- 1-Wire devices that require only a single dedicated contact to operate and power devices
- Exceptional ±15kV (typ) ESD performance on the 1-Wire signal pin (IEC 61000-4-2)
- New SFN packaging that simplifies adding 1-Wire to nonelectronic peripherals



Sensor ID and Calibration Data

AC-Adapter Model Data

Print-Cartridge ID and Authentication

1-Wire Solution Guide

Part	Description	Solution		
		PC-Board ID	Protect IP	Accessory ID
DS2401	64b ROM ID	✔	✔	✔
DS2411	64b ROM ID, 1.5V operation	✔	✔	✔
DS2431	1kb EEPROM	✔	✔	✔
DS2433	4kb EEPROM	✔	✔	✔
DS28E01-100	1kb EEPROM, SHA-1 authorization	✔	✔	✔
DS28EB04*	4kb EEPROM, SHA-1 authorization	✔	✔	✔
DS2502/5/6	1kb/16kb/64kb EPROM	✔	✔	✔
DS2413	2-channel GPIO, 20V/20mA	✔		✔
DS2406	2-channel GPIO, 1kb EPROM	✔		✔
DS28E04-100	2-channel GPIO, 4kb EEPROM	✔		✔
DS18B20	0.5°C accurate temperature	✔		
DS28EA00*	0.5°C accurate temperature, 2-channel GPIO	✔		
DS2460	SHA-1 coprocessor		✔	✔
DS2482-100	I^2C‡ to 1-Wire line driver, single 1-Wire driver	✔	✔	✔
DS2482-800	I^2C to 1-Wire line driver, eight 1-Wire drivers	✔	✔	✔
DS2480B	UART/RS-232 to 1-Wire line driver	✔	✔	✔

*Future product—contact factory for availability.
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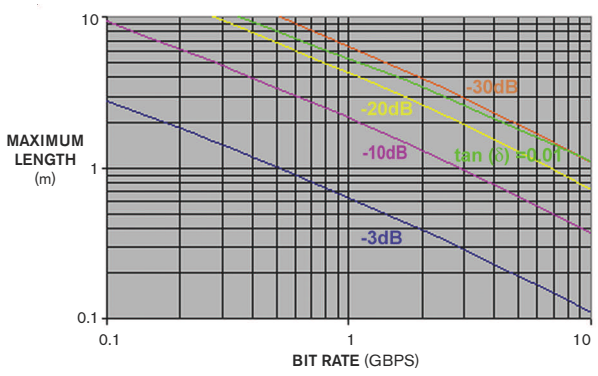

Figure 6 The yellow and green, −20-dB-loss curves contrast the resulting distance that you can drive on FR4 versus a lower loss material, with tan(δ)=0.01 (courtesy Eric Bogatin, PhD).

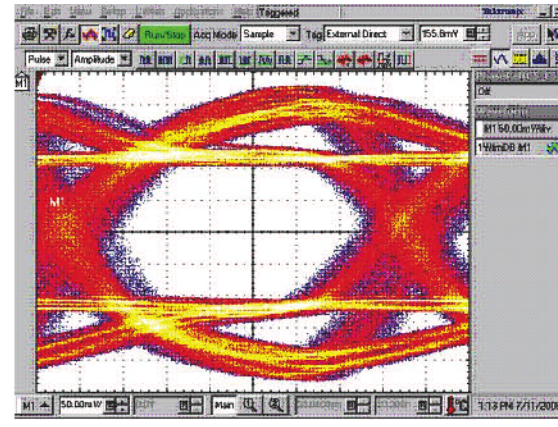

Figure 7 The screen shows the predistorted transmitter eye, using NRZ and PRBS, as it appears at the transmitting driver.

tion sharing between points over their parallel ancestors, because they do not use a separate clock line. **Figure 1** depicts an example layout of a PCI Express interface delivering twice the bandwidth in half the number of interconnects. Other serial-interface standards and data rates are also seeing a significant ramp in use (**Table 1**).

Though standardized protocols facilitate midspan interconnections, as well as modular and interoperable system building blocks, a number of systems architects encapsulate standard protocols or data with signaling, switching, data integrity, and other channel overhead. In these proprietary systems, designers typically use a nonstandard baud rate, which in the past meant they had to implement their design in an ASIC. Now, designers can use FPGAs that accommodate both standard and proprietary serial protocols from 614 Mbps through 6.375 Gbps per lane, including "bonded" lanes in which data spans across multiple serial links, building the aggregate bandwidth by the number of lanes added.

Serial-protocol and baud-rate support, however, is only the tip of the iceberg. The motivation for economic and reliable interconnect does not stop at a silicon vendor's package or business interests. For serial links to succeed and grow in use, the circuitry to transport data must be fairly simple, low-power, and inexpensive. In many instances, the circuitry must fit into legacy chassis, and, for new systems, it must be "evergreened"—backward compatible and externally upgradable through simple plug-ins to quickly increase capacity, performance, and new features for customers, making it more difficult for competitors to take market share.

These economic, strategic, and business interests lend the appearance that the interconnect problem and its solutions are rather boring. To the contrary, it takes a substantial amount of design magic to make excessive interconnect and related problems disappear.

The challenge in most interconnects is to deliver a recognizable signal from the transmitter to the receiver. Most digital designers make a connection with any-sized wire and assume the receiver coincidentally understands the ones and zeros that the transmitter sends. In some cases, having been bitten by the lore of fast edges, designers take great care to either series-damp or parallel-terminate a signal to eliminate false triggering and thresholds. Designers rarely give consideration to impedance, matching, or trace length, because rise and fall times are longer than λ/10, and the loss budget from transmitting to receiving is on the order of −3 dB for most logic. Designers could accomplish greater interconnect bandwidths by simply making buses wider, possibly adding layers to pc boards in the systems, and possibly shipping a sledgehammer with every card to facilitate insertion into hundreds of connector pins at a few ounces of force apiece.

MAKING A SIGNAL DISAPPEAR

Although high-speed serial links may appear to deliver the Holy Grail of insertion force by reducing the number of interconnects by one or two orders of magnitude, they do not come without a price. The amount of consolidated bandwidth requires a high baud rate, mandating speedy rise and fall times. The system must deliver these high edge rates to the receiver by wires that must be insulated from each other. Unlike digital signals of less than 100 MHz, for which the resistance of interconnect wiring is the primary source of signal loss, at high edge rates (high frequency), a "skin effect" occurs. The electric fields in the wire cause electrons to conduct only in the "skin" of the conductor, thus dramatically increasing resistive loss over the bulk cross section of the conductor.

To further complicate matters, this crowding of electrons at the conductor surface produces intense electric fields in the interface between the conductor and the insulating dielectric that has energy-absorbing electrostatic dipoles. This dielectric-loss component dominates resistive loss for interconnect attenuation above 500 MHz for a representative trace geometry and materials set (**Figure 2**). In this example, the dielectric losses are twice that of the resistive loss at 2 GHz and diverge to almost five times the conductive loss at 10 GHz. Digital designers from the "Land of Ohm" must face nature's sleight of hand, in which energy at gigabit speeds becomes lost in a once benign and invisible medium: a conductor's insulation. In addition, familiarity, manufacturability, availability, legacy, reliability, and cost con-

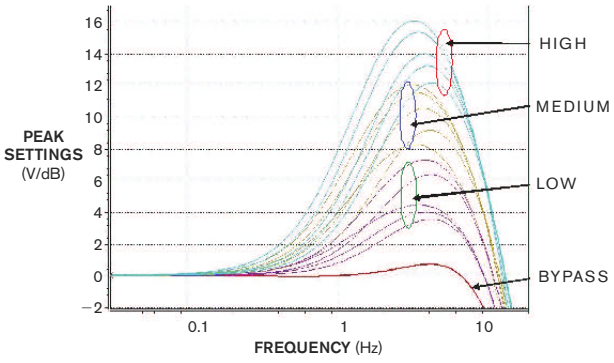

Figure 8 Various receiver-equalizer-gain peaking settings are available in a 90-nm FPGA.

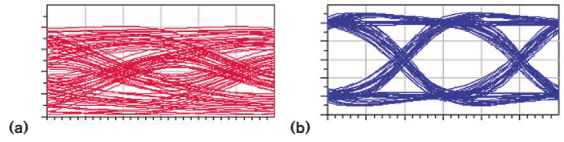

Figure 9 PRBS non-pre-emphasized waveforms show results at an FPGA decision flip-flop without (a) and with (b) optimal equalization.

siderations anchor the constraint of using homogeneous FR4 as the board material of first choice for pc boards and backplanes.

THE MAGICAL PROPERTIES OF VIAS

The curves in **Figure 2** model losses in only a microstrip and do not include the effects from connectors, vias, and impedance discontinuities. Simply adding a 150-mil-long via stub to a signal trace creates 65 dB of further losses at 9 GHz from that of a backplane trace with no vias (**Figure 3**). These signal "suckouts" result from the resonance of the nonconnected portion of the via (the "stub"), yielding an approximate resonant frequency, f, in gigahertz of this one-quarter-wave LC structure in FR4 of: $f=k\times1/(4\times L\times v)$, where k is a correction factor for stray reactance, L is the length of the via stub in inches, and v is the propagation velocity in nanoseconds per inch, which equals 174 psec/in. for FR4.

The novice faces the nonintuitive concept that a barrel of metal lacking an end-to-end electrical connection can resonate with strong electromagnetic fields (**Figure 3a**), thereby annihilating a signal that happens to share a summing node with that via. However, by using the full length of the via as respective input and output ports or by using counterbored or backdrilled vias, designers can model the resulting attenuation curve for an interconnect (**Figure 3b**) and measure the attenuation curve for an 1.25m trace on a GbX-connector-based, backdrilled, FR408 backplane from Molex (**Figure 4**). Although the via may appear to magically vanish, the backdrilling process simply tunes the resonant stub frequency to a substantially higher frequency and out of the information band of the transmitted signal.

After achieving the lowest possible attenuation, what does a signal look like after it traverses the backplane? Inspection of

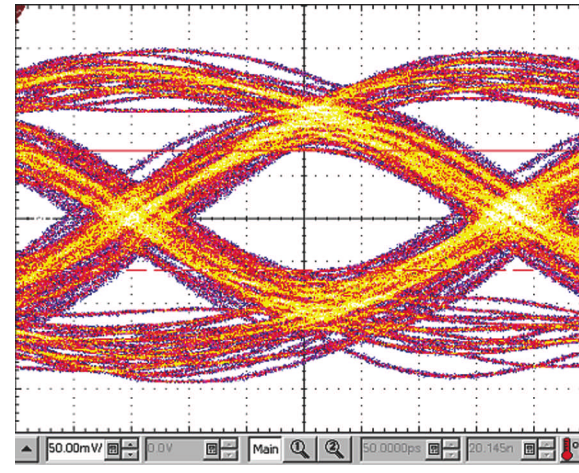

Figure 10 The received PRBS eye at 3.125 Gbps shows results after 18 ft of CAT5 cable and pre-emphasis in an FPGA.

the backplane's attenuation curve in **Figure 4** reveals that low frequencies are moderately attenuated, but there is also a linearly increasing attenuation of the signal with frequency. Severe signal degradation in the higher frequency components of a waveform—namely, in narrow, single-bit pulses and in its rising and falling edges—results in eye closure and ISI (intersymbol interference). For example, when you apply a PRBS (pseudorandom bit sequence) of high-speed NRZ data to a lossy channel, its high-frequency components become attenuated, and the system exhibits reduced amplitudes as pulses shrink to a single-bit width (**Figure 5a**). Rise and fall times are lowpass-filtered to the point at which the signal cannot reach full amplitude before signaling an adjacent complementary bit. The attenuation curve intuitively suggests that a high-frequency PRBS pattern would result in eye closure. The waveform shown in **Figure 5b**, captured at the far end of the FR408 Molex backplane, confirms this suspicion.

Having improved the passive aspects of the attenuation curve, yet having achieved a disappointing closed eye at the receiver, there are two cards left for system designers to play. One is to use a significantly more expensive, higher performance board material that reduces the dominant dielectric-loss component, as the loss tangent of the material specifies. It would reduce the slope of the attenuation curve such that the far end of the backplane might achieve an eye opening. The resulting distance that you can drive on FR4 versus a lower loss material, with $\tan(\delta)=0.01$, contrasts with the yellow and green −20-dB-loss curves in **Figure 6**.

Apart from reducing the slope of the attenuation curve through the use of exotic board materials, designers have a second choice that retains the low-cost, manufacturable aspects of FR4. The trick is to actively distort the frequency response of the overall system such that the serial channel has a flatter effective frequency response. Designers can accomplish this objective by either de-emphasizing low-frequency content or emphasizing high-frequency content of the transmitted and received signals themselves. Multiplying these channel responses and the harmonic content of a predistorted or equalized signal results

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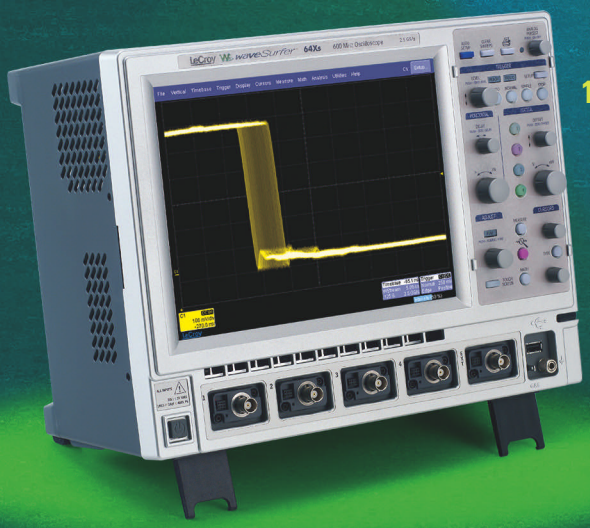

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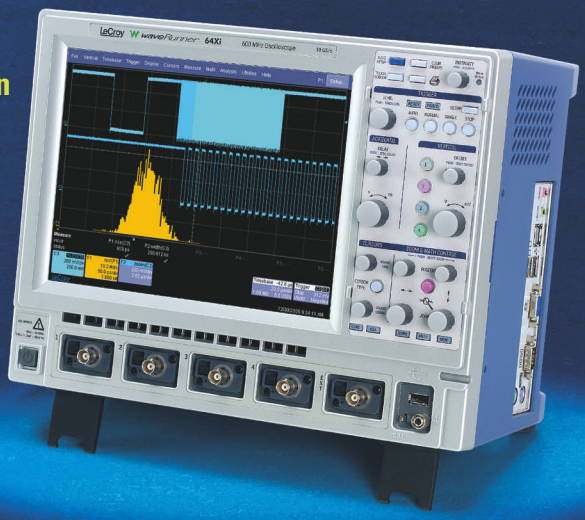

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in a flatter equivalent-frequency response of the signal from transmitter to receiver.

Why de-emphasize low-frequency content? In 1966, RL Johnson of RCA Labs postulated the Johnson Limit: For a given transistor structure and process, the product of breakdown voltage, V_{BR}, and the transistor speed, f_t, is limited. The Johnson Limit for CMOS is about 75V×GHz, meaning that a 3.3V I/O transistor (V_{BR}=4.5V for the process) has about 16 GHz of bandwidth. After considering parasitics, this value is suitable for the edge rates you need in a multigigabit driver for a 90-nm FPGA operating as fast as 6.375 Gbps. The finite headroom on the output driver limits the total voltage compliance. Thus, physics limits the peak-to-peak output. For high-speed, low-jitter output drivers in a 90-nm CMOS process, the intentional predistortion, manifested as high-frequency overshoot, is subject to these limitations, making it appropriate to reduce the low-frequency portion of a waveform to yield the desired ratio of intentional overshoot to "steady-state" levels. This ratio has the overall effect on the launched waveform of decreasing low-frequency components to compensate for the lower attenuation at low frequencies in the FR4 material. In practice, designers use multitap FIR filters for compensation in the transmitter, in which, at 6.375 Gbps, one pretap and two post-taps are sufficient for FR4 (specifically, FR408) backplane applications to 1.25m. The predistorted transmit eye, using NRZ and PRBS, appears at the transmitting driver (**Figure 7**); **Figure 5c** shows the resulting eye at the receiver, after 1.25m of FR4, with

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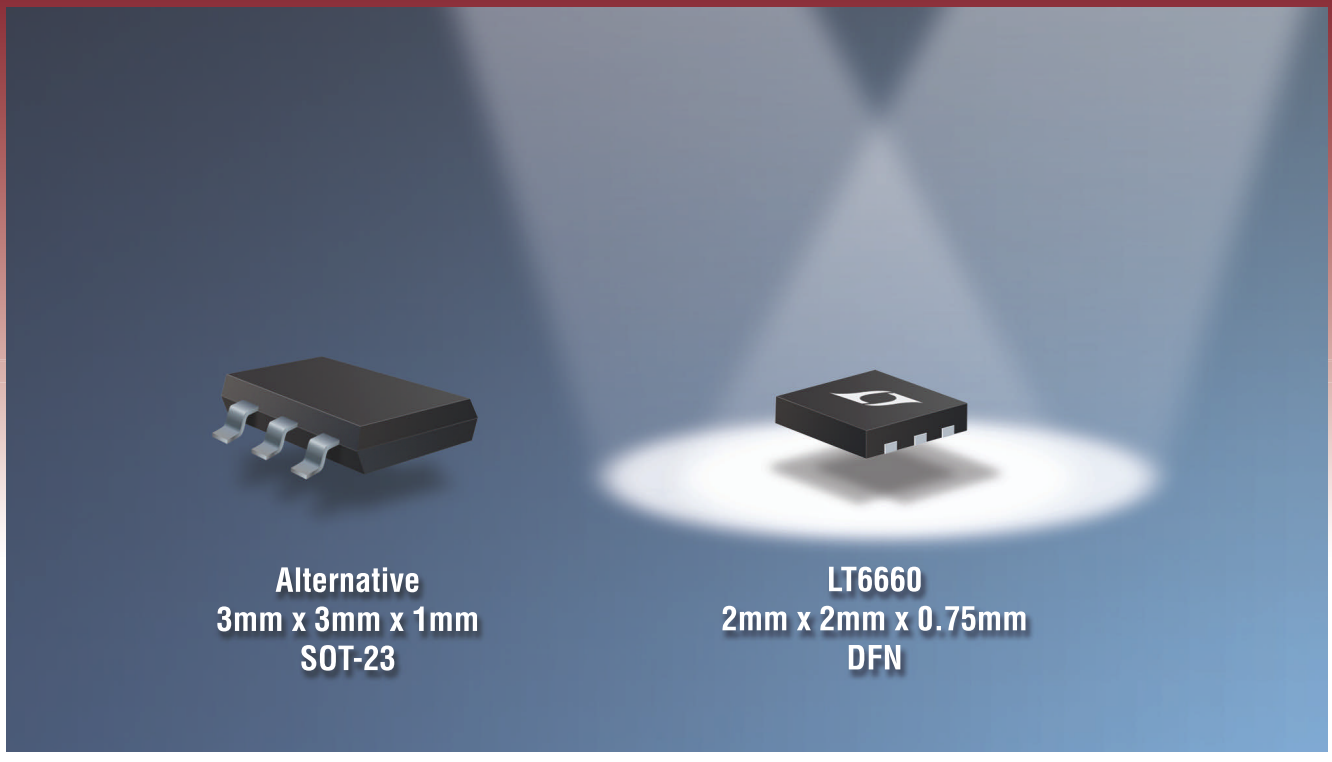
two Molex GbX connectors, a 2m coaxial test cable, and five SMA connectors.

To further open the eye, designers can boost the high-frequency content at the receiver. Here, it is possible for designers to tune (equalize) the response of the receiver amplifier so that it exhibits a higher gain at high frequencies (**Figure 8**). With careful design, system or board designers can dynamically program-in an optimized amount of boost, because excessive boost decreases the SNR of the received signal, and insufficient boost may result in insufficient edge rates and eye opening. **Figure 9** shows the result of having an optimized level of equalization. The **figure** depicts a noncompensated eye and equalized eye, respectively, after a non-pre-emphasized PRBS signal has traversed 42 in. of FR4 at 6.375 Gbps.

SIGNAL-INTEGRITY-OPTIMIZED FPGAs

Designers can adjust pre-emphasis, equalization, and transmitting-drive levels to compensate for the frequency-dependent attenuation effects of connectors, discontinuities, and losses in a backplane, or even those of cable. **Figure 10** shows 18 ft of standard RJ45-connectorized Category 5 wire at 3.125 Gbps using FPGA pre-emphasis capabilities. To illustrate, Altera's Stratix II GX 90-nm FPGA with multigigabit transceivers has more than 5000 possible combinations, making optimization of signal integrity a nightmare in systems with multiple and varying channel lengths or properties. During the design phase of the system, designers can measure s-parame-

References 1/2 Off



Tiny 20ppm/°C Precision References. No External Components Required.

The LT®6660 is the first precision series voltage reference in a tiny 2mm x 2mm DFN package, reducing board area to less than half of a SOT-23. Requiring no output capacitor, the LT6660 is perfect for space-constrained designs. Despite its size, the LT6660 doesn't compromise performance, guaranteeing less than 20ppm/°C drift, 0.2% initial accuracy and consuming a mere 145µA. Operating with input voltages up to 30V and sourcing up to 20mA, the LT6660 is also ideal as a precision voltage regulator.

Ultra-Small References

Part Name	LT6660H	LT6660J	LT6660K
Output Voltage (V)	2.5, 3, 3.3, 5, 10V	2.5, 3, 3.3, 5, 10V	2.5, 3, 3.3, 5, 10V
Accuracy (Max.@25°C)	0.20%	0.40%	0.50%
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Output Noise (0.1Hz ≤ f ≤ 10Hz)	4ppm (p-p)	4ppm (p-p)	4ppm (p-p)
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ters for each card-slot position. They can then run the PELE (pre-emphasis-and-equalization-link-estimator) program using The MathWorks' (www.mathworks.com) Matlab code, which incorporates an FPGA-multigigabit-transceiver-specific model, to determine the optimal pre-emphasis, drive level, and equalization for each channel in the system. The dynamic configurability of an FPGA then comes into play. Designers can read the backplane-slot ID and then change settings to optimize the eye for each blade position without altering the configuration of the FPGA core. Designers can enable other system capabilities by using a small controller in the FPGA to automate the receiver equalizer, making it adaptive to system, environmental, and component variations.

FPGAs are well-suited to providing access to the density and performance that advanced process nodes offer, enabling system designers to develop highly integrated SOCs (systems on chips) in the shortest amount of time. FPGA vendors also offer debugged protocol IP, thus reducing R&D. FPGA packaging and design techniques mitigate simultaneous-switching-noise effects on all I/O, including serial links, allowing designers to use a large number of parallel I/O for devices including external memory and ASICs. To address the concerns of interconnecting large amounts of information, either intrasystem or intersystem, FPGAs are available now with large counts of multigigabit serial I/O. These high-speed, multigigabit transceivers have paced the system need of remaining on low-cost FR4 materials, and provide lower bit-error rate, higher interconnect bandwidth, and lower power dissipation than discrete serializer/deserializer devices.

As CMOS-process nodes continue to shrink below 100 nm, most, if not all, systems will use an FPGA with multigigabit serial interconnects or a structured ASIC for integrating systems onto a chip. The advanced signal-conditioning techniques that this article presents, which are available in high-end FPGAs, will appear rather mundane in the coming decades, particularly as device speeds push into the tens of gigahertz of operation and as the magical tricks of signal-integrity wizards become common knowledge. EDN

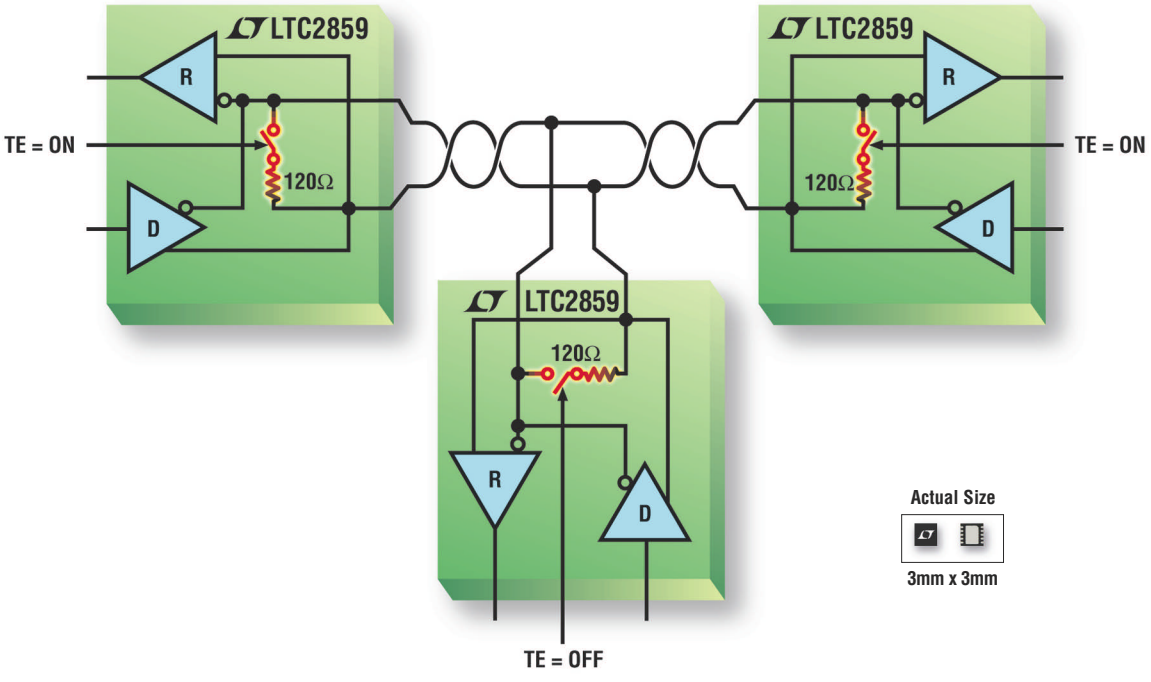
ACKNOWLEDGMENTS

The author would like to thank Steve McKinney at Mentor Graphics; Eric Bogatin at www.bethesignal.com; Gourgen Oganessyan at Molex; and Leonard Dieguez, Tina Tran, Mark Flanigan, Naresh Raman, Venkat Yadavalli, Samson Tan, Michael Woo, and Dave Greenfield at Altera.

AUTHOR'S BIOGRAPHY

Andy Turudic is a senior manager for Altera's high-end-FPGA-product line. He is currently investigating advanced, high-speed applications and signal integrity of multigigabit FPGAs in backplanes and cables. He has been involved in research, development, applications engineering, and marketing of high-speed serial communications, PLLs, and mixed-signal devices for more than 26 years. He holds a bachelor's degree in electrical engineering from the University of Windsor (Windsor, ON, Canada), holds eight US patents, and is a senior member of the IEEE.

RS485 with Switchable Termination



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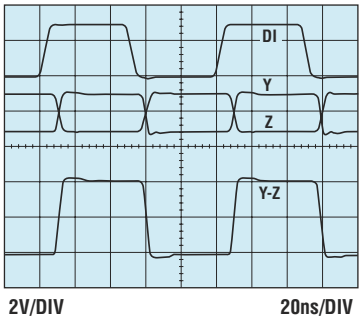

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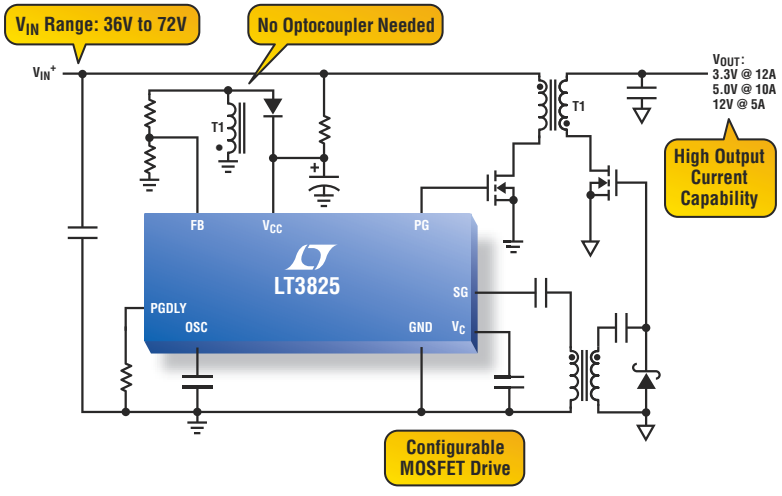

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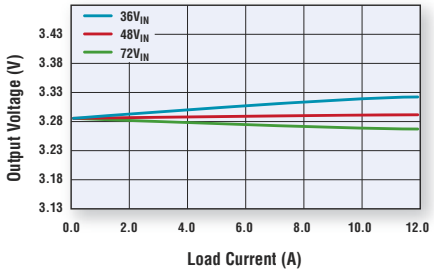

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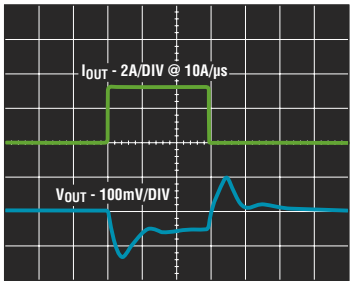

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DESIGN NOTES

AdvancedTCA Hot Swap Controller Monitors Power Distribution

Design Note 397

Mitchell Lee

Introduction

AdvancedTCA® is a modular computing architecture developed by the PCI Industrial Computer Manufacturers Group for use in central office telecom environments. PICMG® 3.0 defines, among other things, the electrical and mechanical attributes of the backplane, connectors and removable cards in these –48V systems.

Each removable card, or front board, is designed for live insertion into a working system. A power draw of up to 200W per front board is allowed, placing the maximum load current in the 4A to 5A range.

Card-centric inrush limiting and quantitative current and voltage monitoring are highly desirable to sanitize the incoming battery feeds, minimize power plane disturbances, allow for budgeting power consumption and permit failure prediction in an otherwise functional system. The LTC®4261 Hot Swap™ controller provides these features. Also included is a digital interface for controlling the functions of the LTC4261, and for reading the current and voltage measurement registers.

Circuit Solutions

Figure 1 shows a complete circuit designed to handle up to the maximum available power. The LTC4261's accurate current limit is set to provide at least 5.5A under all conditions, a comfortable margin for 200W, yet trips off just under 7A to preserve fuse integrity in the presence of nuisance overloads. At insertion the LTC4261 allows contact bounce to settle, then soft starts the load using a ramped current. Inrush current is increased gradually to a few hundred milliamperes and held there until the MOSFET is fully on.

Current is monitored by the SENSE pin and an 8mΩ shunt resistor. Direct measurement of the current is possible via the I^2C port, with 10-bit resolution and 8A full scale.

Cutting Diode Dissipation

ATCA's redundant –48V power feeds are combined on-card with ORing diodes. At 5A current consumption even Schottky rectifiers present a serious problem in terms of both voltage drop and power dissipation: a conducting pair drop more than 1V and dissipate 6W. Following the diode manufacturer's recommendations, 8 square inches of board area are needed to satisfy the heat sinking requirements.

Diode dissipation, voltage loss and board area is reduced in Figure 1 by using MOSFETs as active rectifiers with the LTC4354 diode OR driver. Total dissipation is cut to less than 1W for two conducting "diodes" at maximum load.

Zero Volt Transient

The so-called Zero Volt Transient requirement is a legacy of earlier telecom equipment standards stipulating uninterrupted system operation during the course of a 5ms input voltage dropout. An energy of 1J is needed to sustain a 200W load during this interval.

The accepted method of energy storage to satisfy the 1J requirement is a bulk reservoir capacitor which is charged through resistors. This technique dictates the use of bulky high voltage storage capacitors, such as 100V (or rare 80V) rated units which can handle the maximum input voltage of 75V. Since the zero volt transient test commences at 44V, nothing is gained by storing a higher voltage. Compact 50V capacitors are used instead, by limiting the charging voltage with a simple zener-transistor circuit.

The ATCA connector pin configuration presents a special design challenge. Here extraction is inferred from the difference between each ENABLE and its associated VRTN, thereby ignoring input dropouts. A PNP transistor pulls up on $\overline{EN}$ in the event of an ENABLE disconnect, shutting down the LTC4261 and permitting safe extraction with no connector damage. During a zero volt transient, no signal reaches the $\overline{EN}$ pin; power flows uninterrupted to the load when the input voltage recovers.

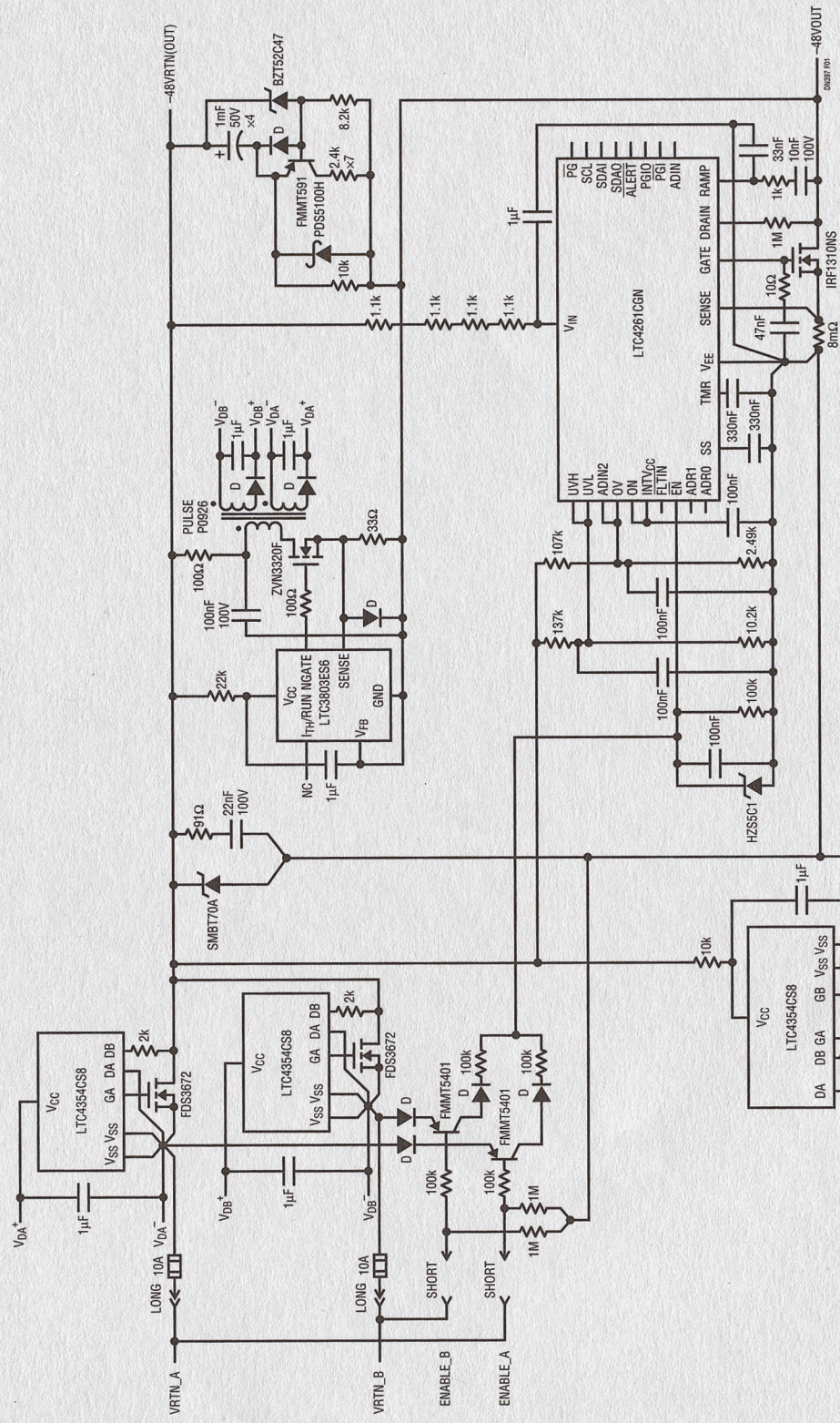

Figure 1. AdvancedTCA Hot Swap Controller with I²C Current and Voltage Monitor

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READERS SOLVE DESIGN PROBLEMS

"Brick-wall" lowpass audio filter needs no tuning

Diego Puyal and Pilar Molina, University of Zaragoza, Zaragoza, Spain

When a system's specifications call for a lowpass filter with a steep frequency-cutoff characteristic, an engineer can opt for a "brick-wall"-filter design that features a sharp transition band. For example, in an FM stereophonic-broadcast system, the lowpass filter in the baseband audio's left and right channels should have a −3-dB cutoff frequency of at least 15 kHz, a passband ripple of less than 0.3 dB, a stopband start frequency of at least 19 kHz, a stopband attenuation greater than 50 dB, and identical phase response for both channels.

The filter should provide adjustable gain to maximize SNR at the audio processor's first stage. The filter's frequency response should also include a notch at 19 kHz to achieve maximum attenuation at the FM-subcarrier pilot-tone frequency and thus minimize phasing problems. To reduce manufacturing costs, the filter should require no in-process adjustments. Conventional analog active-filter designs cannot meet these goals at reasonable cost and complexity without time-consuming adjustments. This Design Idea outlines an active-filter-synthesis approach that reduces a filter's sensitivity to passive-component tolerances and enables construction of inexpensive, high-order and highly selective filters.

The design process begins with selection of an appropriate passive-filter topology—in this example, a seventh-order elliptic filter with 50Ω input and output impedances (**Figure 1**). Setting the beginning of the stopband frequency span at 18.72 kHz produces a notch at the 19-kHz stereo-pilot frequency. Using the following **equation** to transform each component's impedance leaves the filter's amplitude-versus-frequency response characteristics unaltered.

$$Z'(s)=\frac{k}{s}\times Z(s).$$

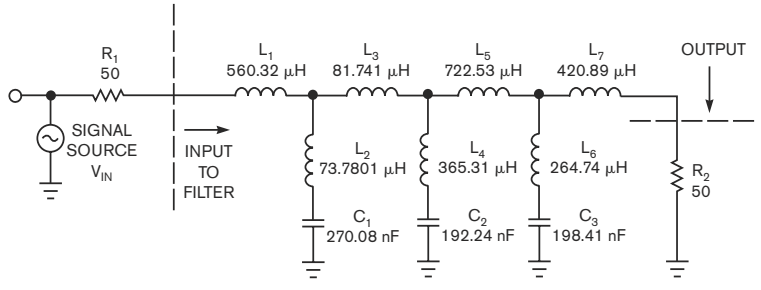

Figure 1 This seventh-order, elliptic, lowpass, passive-filter prototype features a 15-kHz cutoff frequency and stopband rejection exceeding 50 dB.

DIs Inside

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As a result of the transformation, all resistors undergo transformation into capacitors, and adjusting the value of parameter k yields reasonable capacitance values for using 10%-tolerance parts. In this instance, select a value of 2.2 nF for C_1':

$$k=\frac{1}{R_1\times C_1'}.$$

Inductors transform into resistors, and using 2%-tolerance or better components meets the circuit's requirements. Capacitors transform into "supercapacitors" whose impedance exhibits a $1/s^2$ dependence:

$$Z'(s)=\frac{k}{s}\times\frac{1}{C_i s}=D_i'\times\frac{1}{s^2}.$$

Selecting a topology for a passive filter that contains the maximum number of inductors and references all capacitors to ground yields a transformed filter that consists of many resistors, several supercapacitors, and only two capacitors. You cannot obtain a supercapacitor as an off-the-shelf component, but its electrical analog comprises a few operational amplifiers and resistors (**Figure 2**). The following **equation** defines the gyrator's input impedance, Z_{IN}, with respect to ground:

$$Z_{IN}=\frac{Z_1\times Z_3\times Z_5}{Z_2\times Z_4}.$$

Selecting $Z_1=Z_3=1/Cs$ in the **equation**, setting capacitor value C at 2.2 nF, replacing impedances Z_2 and Z_5 with R=11 kΩ, and setting $Z_4=R_4$ yield a solution for D_i':

$$D_i' = \frac{C^2}{R_4}.$$

Figure 2 shows the filter's final schematic. Potentiometer R_1 adjusts the overall gain, and connecting resistors R_2 and R_{26} in parallel with capacitors C_1 and C_8 prevents dc blocking. The finished filter design uses medium-tolerance resistors, only eight capacitors, and two LF347 quad operational amplifiers—few amplifiers for a seventh-order active filter that requires no component adjustments to meet its specifications. Thanks to the design's precise implementation of the pilot-tone-rejection notch, the filter's measured attenuation at 19 kHz exceeds 60 dB. EDN

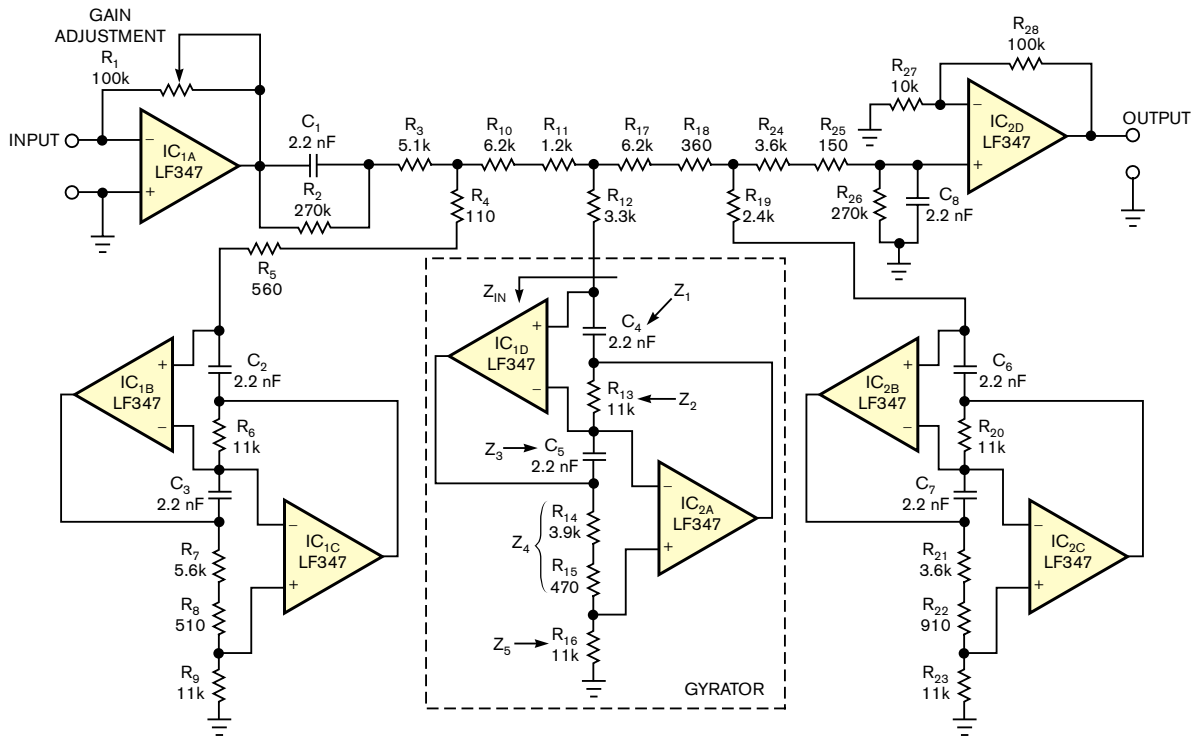

Figure 2 The finished circuit design eliminates inductors and substitutes gyrators as "supercapacitors." Using medium-tolerance components and quad op amps to reduce component count minimizes circuit cost.

Fast-settling picoammeter circuit handles wide voltage range

Rob Whitehouse, Analog Devices, Wilmington, MA

Evaluating analog switches, multiplexers, operational amplifiers, and other ICs poses challenges to IC-test engineers. A typical test scenario requires application of a test or forcing voltage to a device's input and measurement of any resultant leakage and offset currents, often at levels of 1 pA or less. In contrast to slow and expensive commercially available automated testers, the low-power measurement circuit in **figures 1** through **3** can force a wide range of test voltages and offer fast settling to maximize device-test throughput. Extensive use of surface-mounted components minimizes

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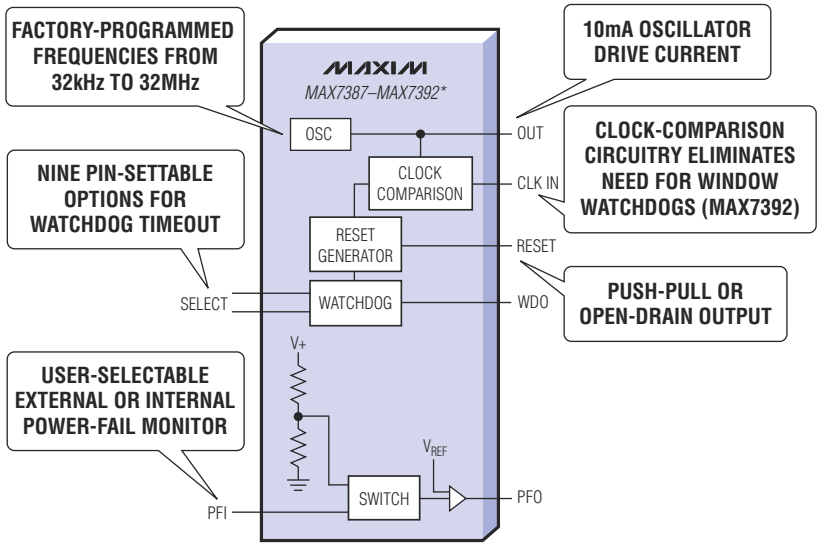

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MAX7388	✓			✓			8-µMAX, 8-DIP
MAX7389	✓	✓					8-µMAX, 8-DIP
MAX7390	✓				✓		8-µMAX, 8-DIP
MAX7391			✓	✓	✓		8-µMAX, 8-DIP
MAX7392*	✓		✓	✓		✓	10-µMAX

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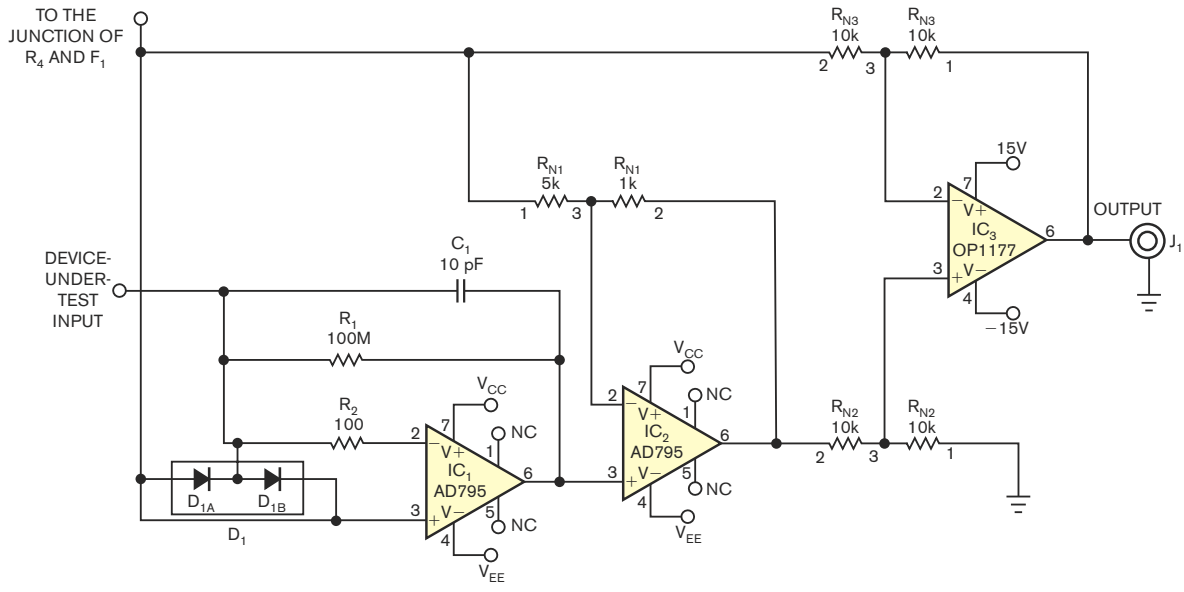

NOTE: R_{N1}, R_{N2}, AND R_{N3} ARE VISHAY MPM-SERIES RESISTOR NETWORKS.

Figure 1 This IVC uses a feedback-ammeter topology, which subtracts an unknown current from a feedback current and delivers an output voltage proportional to the unknown current.

its pc-board-space requirements and allows packaging of multiple measurement circuits close to the test fixture.

The circuit comprises a forcing-voltage buffer/amplifier, a floating-rail power supply, and an IVC (current-to-voltage converter). Applying a forcing voltage to a device under test induces leakage current, which the circuit converts to an output voltage proportional to the leakage current. In a conventional IVC, the current to be measured develops a voltage across a shunt resistor. The IVC uses a feedback-ammeter topology in which operational amplifier IC_1, an Analog Devices AD795, subtracts an unknown current from a feedback current and delivers an output voltage proportional to the unknown current (**Figure 1**).

In this design, the input's dc resistance consists mostly of R_2 and IC_1's effective input resistance, or slightly more than 100Ω at dc. At frequencies in the power-line range of 50 to 300 Hz, the circuit's ac impedance averages approximately 10 kΩ, or 1000 times less than a typical shunt-resistance IVC's input resistance of approximately 10 MΩ. The circuit's 100-MΩ feedback resistor, R_1, provides a current-to-voltage-conversion ratio that exceeds the shunt-conversion ratio by a factor of 10. This design settles much faster and provides better interference rejection at power-line frequencies than shunt converters. It also reduces unwanted voltage-divider effects when testing operational amplifiers' input currents.

R_1 produces a current-to-voltage-conversion ratio of 100 µV/pA. Amplifier IC_2, an AD795, provides an additional voltage gain of 10, boosting the ratio to 1 mV/pA and reducing the effect of errors that differential ampli-

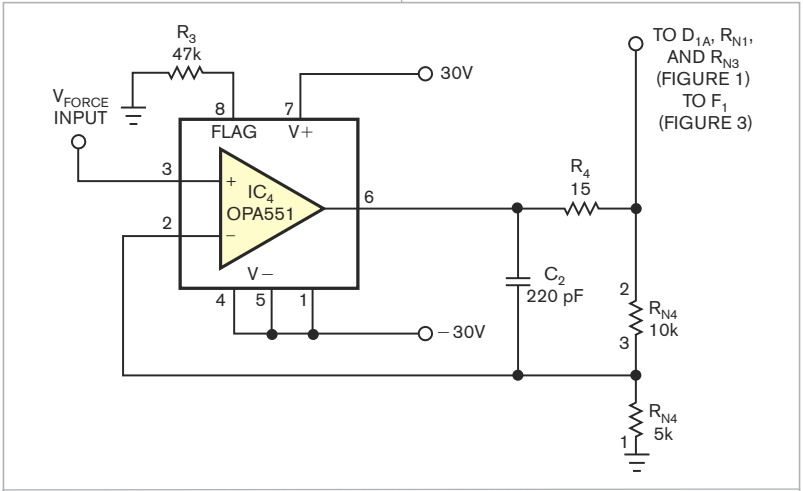

Figure 2 A gain-of-three high-voltage amplifier derives forcing voltages as high as ±22V from voltages of ±7V from test equipment.

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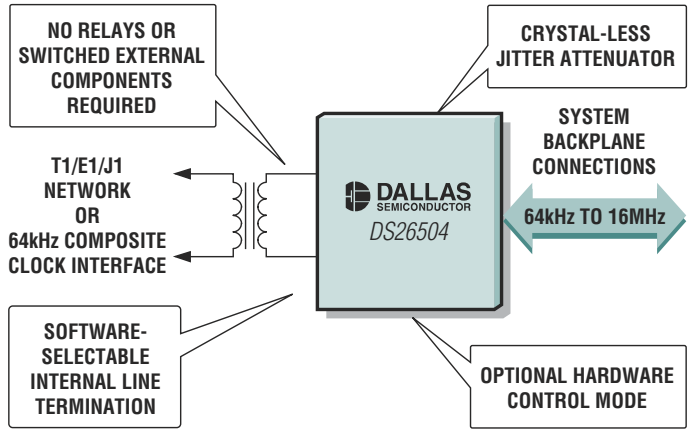

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DS26502L		✓		✓	✓	✓	✓			0 to +70	16.04
DS26503L				✓	✓	✓	✓			0 to +70	11.23
DS26504LN	✓	✓	✓	✓	✓	✓	✓	✓	✓	-40 to +85	20.17
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fier IC_3's CMRR (common-mode-rejection ratio) introduces. Differential amplifier IC_3, an OP1177, subtracts the forcing voltage from the IVC's output and provides a ground-referenced output signal.

A back-to-back pair of BAV199 diodes, D_{1A} and D_{1B}, protects IC_1 from voltage overloads by shunting high currents to the forcing-voltage amplifier, IC_4, and its protective fuse, F_1. When the forcing voltage rapidly slews from one value to another, the diodes greatly improve the IVC's settling time by providing high-drive currents during high-slew-rate intervals.

Operating from ±30V supply rails, a lightly compensated, gain-of-three, high-voltage OPA551 amplifier, IC_4, derives forcing voltages as high as ±22V from ordinary ATE (automatic-test-equipment) voltages of ±7V (**Figure 2**). In case of a catastrophically shorted device under test, fuse F_1 prevents further damage by limiting fault current from IC_4, which can deliver as much as 380 mA of short-circuit current.

The output of IC_4 also drives a regulator circuit that produces ±5V floating-power-supply voltages referenced to the test-input forcing voltage (**Figure 3**). This part of the circuit dissipates less than 100 mW of power with ±30V supplies. Vishay/Siliconix (www.vishay.com) SST505 JFET constant-current regulator "diodes" Q_1 and Q_4 provide 1-mA constant-current sources, which transistors Q_2 and Q_3 buffer. Each current-regulator diode carries a 45V maximum rating, and the buffers provide overvoltage protection by limiting the voltages applied across the diodes to approximately 3V.

Applying 1 mA to resistors R_5 and R_6 develops the ±5V rail voltages. Diodes D_2 and D_3 compensate for the base-emitter-voltage drops across emitter followers Q_{6B} and Q_{7B}. Transistors Q_{6A} and Q_{7A} provide overvoltage protection when a defective device under test short-circuits its power supply to the IVC's input node. Transistors Q_5 and

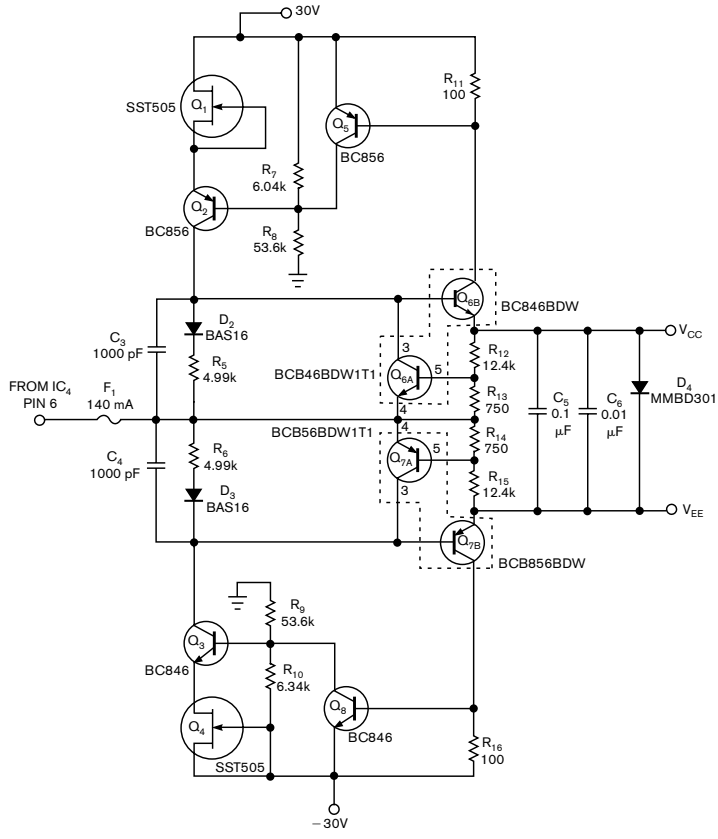

Figure 3 This floating-regulator circuit produces ±5V floating-power-supply voltages V_{CC} and V_{EE} referenced to the test input's forcing voltage.

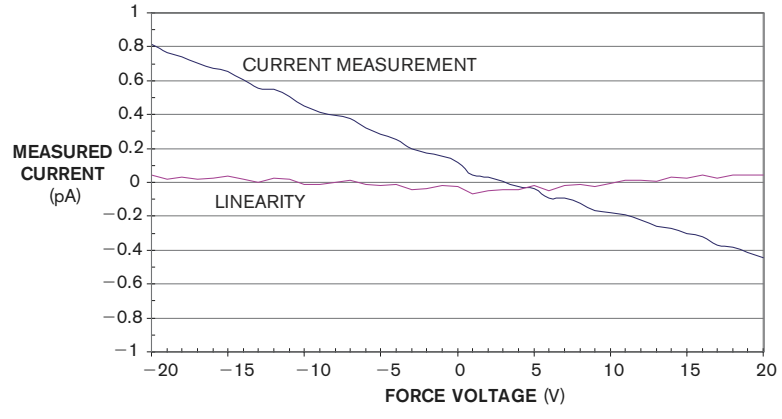

Figure 4 Over a ±20V forcing-voltage span, the circuit produces an unloaded-output current-measurement error of −31 fA/V.

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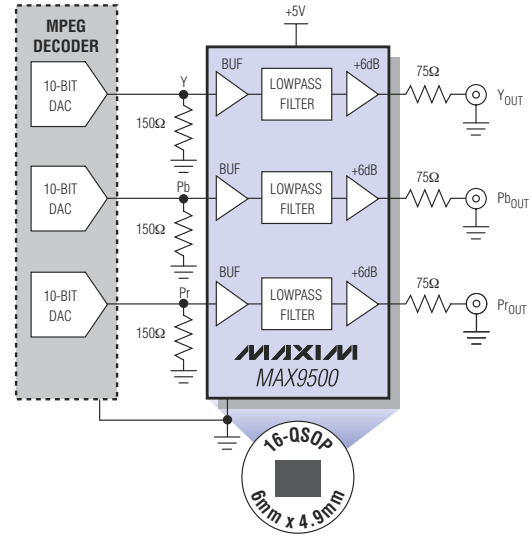
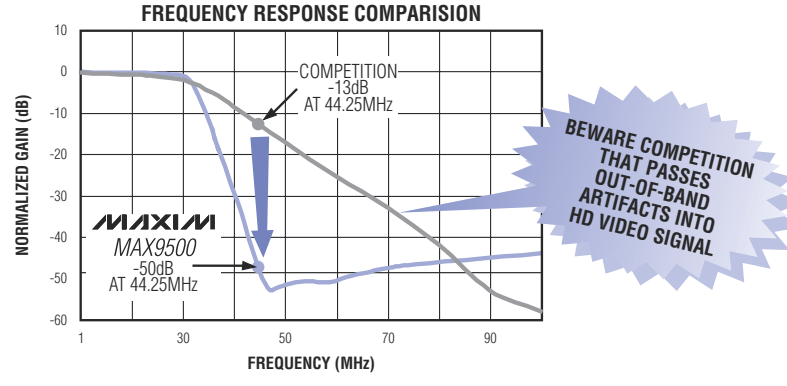
  - 30MHz Passband with ±1.5dB Flatness
  - 50dB Attenuation at 44.25MHz
- Single +5V Operation (MAX9500) or Dual ±5V Operation (MAX9501)
- Eliminate Input and Output Capacitors that Distort Video Signals

Additional Features

- 9ns Group-Delay Variation
- Sink-and-Source Output Current
- Drive 150Ω Directly to Ground
- High-Impedance Input Buffers Interface with Current-Output DACs





Part	No. of Channels	Supply Voltage (V)	30MHz Flatness (dB)	Attenuation at 44.25MHz (dB)	Attenuation at 74.25MHz (dB)	Package
MAX9500	3	+5	±1.5	50	40	16-SO/QSOP
MAX9501		±5				

MAXIM

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Q_8 limit the floating supplies' output currents by shunting the current diodes. Diode D_4 protects against polarity inversion of the floating-supply rails during unusual start-up conditions.

In operation, the circuit delivers an output of 0.999V/nA over a ±4-nA full-scale input range at an effective transresistance of 1 GΩ. The circuit's output offset corresponds to approximately 143 fA. Beyond the forced-voltage span of ±22V, the floating-supply-rail voltages begin to saturate, the input-CMRR limitations of IC_3 become evident, and the IVC's output voltage becomes nonlinear. **Figure 4** shows the circuit's current-measurement error of −31 fA/V from the circuit's unloaded output over a ±20V forcing-voltage span. The differential amplifier comprising IC_3, R_{N2}, and R_{N3} contributes most of the circuit's gain, and IC_1's low input-bias current contributes to the low offset error. Output linearity over the ±20V forcing-voltage range averages 111 fA p-p.

THE CIRCUIT'S SLEW-RATE CAPABILITY VARIES CONSIDERABLY, BUT IN GENERAL THE OUTPUT FAITHFULLY SLEWS THE ENTIRE 40V FORCING-VOLTAGE SPAN IN 100 µSEC OR LESS.

The circuit's slew-rate capability varies considerably, but in general the output faithfully slews the entire 40V forcing-voltage span in 100 µsec or less as D_1 drives the device under test. Once the high-slew period completes, the IVC comes out of saturation, and its output becomes an exponential voltage with a time constant of 1 msec. The output settles to 100 fA in approximately 10.6 msec. Under no-load conditions, the circuit consumes approximately 10.2 mA from the ±30V supplies and 400 µA from the ±15V supplies. The prototype circuit's layout occupies approximately 1.5 $in.^2$ on a single-sided pc board, and placing components on both sides of a double-sided board would reduce the area to 1 $in.^2$ For best performance, the layout must include guard rings around the input terminal and all traces attached to Pin 2 of IC_1. The circuit's size allows its placement on a device-under-test fixture to minimize lead lengths and power-line-induced electromagnetic interference. Although able to measure currents as small as 1 pA, the circuit can accommodate larger currents by reducing the value of R_1. EDN

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...and less cost

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Better technology = more efficiency

The new D1U-W-1600-12-HC has been designed using the latest technologies to be the most efficient 1600W power supply available. Created to service new generation blade servers, it achieves its slim (1U) proportions with a multi-phase interleaved boost PFC, planar transformer and choke, and multi-layer PCBs to replace cabling.

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Product Specifications		D1U-W-1200-12	D1U-W-1600-12
Total Output Power (W)		1200W/900W	1600W/1200W
Output Voltage	Vdc1	12	12
	Vdc2	3.3 or 5	3.3 or 5
Rated Output Current	Iout-1 (A)	98/73	131/98
	Iout-2 (A)	6/4	6/4
Input Voltage Range (VAC)		90-264	90-264
Isolation Voltage	Pri-Sec	3000Vrms	3000Vrms
	Pri-Chassis	1500Vrms	1500Vrms
PFC		Yes	Yes
Current Share		Active	Active
Efficiency		92%	92%
Features	HotPlug	Yes	Yes
	I^2C	Yes	Yes
	EMI Class	Class A	Class A
	Airflow Direction	Back or Front	Back-Front
	Input Connector	IEC 320 C15	IEC 320 C20
	Output Connector	FCI PowerBlade #51732-021	FCI PowerBlade #51732-021
Dimensions (WxLxH)	Inches	4.75 x 12 x 1.6	4.75 x 12 x 1.6
	mm	120,6 x 305 x 40,7	120,6 x 305 x 40,7
Datasheet Name		D1U-W-1200-12	D1U-W-1600-12

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productroundup

SENSORS AND TRANSDUCERS

Color-sensor assembly uses 64 photodiodes

Providing a reflective sensor that can sort or match surfaces by color, the OPB780 reflective-color-sensing assembly has a high-resolution digital measurement of the red, green, and blue components of the light a surface reflects. The device's white LED illuminates the surface of an object and receives the reflected light with an eight-row-by-eight-column-photodiode array. The array comprises four selectable groups of red-, green-, blue-, and clear-filtered photodiodes, and each group integrates the reflected filtered light to minimize nonuniformity. A light-to-frequency converter in the CMOS monolithic sensor allows direct communication with a microcontroller, creating a square-wave output with a frequency directly proportional to light intensity. The OPB780 color sensor costs $11.04 (10,000).

Optek Technology, www.optekinc.com

Light-to-digital sensor uses a 50/60-Hz rejection filter

Combining a photodiode, a current amplifier, a 50/60-Hz rejection filter, a 15-bit ADC, and an I²C output, these integrated light-to-digital sensors suit backlight control, improving battery life and panel visibility. Able to sense ambient light from 380 to 770 nm, the ISL29001 and ISL29002 reject unwanted infrared radiation and convert light intensity to the I²C digital-output signal with low power consumption and human-eye sensitivity. The ISL29001 comes in a DFN-6 package and costs $1.30; the ISL29002 comes in a DFN-8 package and costs $1.39.

Intersil Corp, www.intersil.com

Interface IC features on-chip antialiasing

Featuring a wide-range programmable gain, programmable filters, a 12-bit ADC, and on-chip antialiasing, the MSCPSI sensor-interface IC interfaces voltage-output sensors to a digital-signal output. Using an internal PICmicro to control these features, the device also has a low-noise preamp configurable to differential or single-ended mode. Users can select differential-power modes through serial ports using the on-chip bias section. Additional features include a temperature sensor, a dc-offset-adjustment circuit, and a four-input multiplexer for the ADC. Requiring a single supply from 3.3 to 5.5V dc, the device has a typical 3-mA operating current in low-power mode. The MSCPSI costs $9.90.

Mixed Signal Integration, www.mix-sig.com

Ambient-light sensors suit automotives, consumer electronics

These ambient-light sensors come in surface-mount 0805, leaded 5-mm flat-top, and leaded 3-mm packages. Using a two-pin connection, the sensors reduce power consumption by controlling keypad backlights and by adjusting the brightness of the LCDs in consumer electronics. In automotive applications, the sensors enable automatic headlight control, tunnel sensors, and displays that automatically adjust to changes in ambient brightness. As phototransistors, these sensors require no external amplifiers. The sensors cost 25 cents (1 million).

Vishay, www.vishay.com

Finger-tip sensors measure pressure to 10 lbs

The FingerTPS finger-tip tactile-pressure sensors measure the pressure that a user exerts. Users wear the sensor on their finger tips and palms while performing the measured action. Based on capacitive-sensor technology, the device can measure pressure to 10 lbs in 0.1-lb

productroundup

SENSORS AND TRANSDUCERS

increments. A stretchable fabric mounting provides a tight fit to a user's fingers and measures less than 2 mm thick. Evaluation kits for a single-hand system with two sensors cost $2995, a two-hand evaluation kit costs $3995, and additional sensors cost $495 each.
Pressure Profile Systems, www.pressureprofile.com

SST has accurate ambient- and external-temperature rates

The EMC1102 and EMC1152 temperature-sensing devices comply with Intel's high-speed, single-wire SST (simple-serial-transport) bus. Both dual-temperature sensors feature ambient- and external-temperature rates of ±1°C. The EMC1152 measures five supply voltages in desktop PCs, enabling it to monitor supply-voltage rails on the motherboard. The EMC-1102 comes in an MSOP-8 package and costs 90 cents (10,000); the EMC-1152 comes in an MSOP-10 and costs $1.20 (10,000).
SMSC, www.smsc.com

Design kit features five sensors for accurate temperature sensing

Five thermal-ribbon, thermal-tab, and bolt-on RTD (resistance-temperature-detector) sensors in the non-invasive-sensor-design kit allow users to accurately sense temperature in places normally requiring drilling or tapping a sensor. Features include a miniature TempTran temperature transmitter with 4- to 20-mA output; a silicone-stretch tape; and a design-guide booklet containing a start-up guide, technical specifications, and white papers. The non-invasive-sensor-design kit costs $189.
Minco, www.minco.com

TEST AND MEASUREMENT

PCI-digitizer cards stream at 200M samples/sec

Based on the UF2 series carrier card, the PCI-digitizer cards use a 66-MHz/32-bit PCI PCI-X bus continuously transferring data to the host PC at 225M samples/sec. Using multiple 8-bit ADCs, the cards have a 100M-sample/sec maximum sampling rate or 200M samples/sec in interleave mode. Each card comes with a 64-Mbyte signal memory. Free downloads of future OS-version drivers and drivers for MatLab, LabView, VEE, DasyLab, and LabWindows/CVI are available. Two- and four-channel cards cost $4290 and $6990, respectively.
Strategic Test Corp, www.strategic-test.com

Chassis integrates PCI Express technology, MXI-Express controller

Integrating PCI Express technology into the PCI-1033 chassis reduces costs by incorporating the MXI-Express controller into the chassis, as well. The MXI-Express controller allows 110-Mbps sustained throughput to the

TEST AND MEASUREMENT

host PC. Additional features include the vendor's LabView graphical development environment, LabWindows/CVI software for ANSI C development, SignalExpress interactive-measurement software, and the vendor's TestStand test-management software. The PCI-1033 chassis costs $999.

National Instruments, www.ni.com

Upgrade for debugging tool improves USB performance

Updating the J-Scan boundary-scan debugging and programming tool, Version 2.1 allows circuit designers to facilitate early test development, shortening the development cycle and prototyping process. Version 2.1 communicates to the target through a USB 1.1- and USB 2.0-compatible interface running in high-speed or full-speed modes, providing a 10 times better performance than previous versions. The tool also supports SPI flash programming. J-Scan Version 2.1 costs $1895.

Macraigor Systems LLC, www.macraigor.com

EMBEDDED SYSTEMS

Software-radio transceiver boosts FPGA, memory, and ADC resources

Providing software-radio-transceiver functions suiting IF- or RF-communication systems, the Model 7142 PMC module includes dual Virtex-4 FPGAs, four ADCs, and 50% more memory than previous models. Digitized RF signals from the four 14-bit, 125-MHz ADCs pass into a Virtex-4 SX55 FPGA or route to other module resources, including a dc to 160-MHz digital upconverter; a 16-bit, 500-MHz DAC; 768 Mbytes of DDR2 SDRAM; and a Virtex-4 FX FPGA-handling I/O. An FX device features a PCI-bus interface with a nine-channel DMA controller. A VITA 42-compliant XMC dual 4-Gbyte serial interface supports switched fabrics. Vir-

tex-4 SX55 functions include transient capture, advanced triggering modes, and waveform playback. The devices also offer control and programming interfaces to the other onboard resources. Available in PCI, 3U, 6U CompactPCI, and PMC conduction-cooled versions, the Model 7142 PMC module costs $13,500.
Pentek, www.pentek.com

Flat-panel touchscreen computers use no moving parts

Able to function over 0 to 50°C without fans or other moving parts, the SeaPAC flat-panel touchscreen-computer family uses a low-power 1-GHz Celeron M processor. Features include a 10/100 Base-T Ethernet, two serial ports, and three high-speed USB 2.0 ports. The vendor's SealI/O data-acquisition modules allow local and remote I/O expansion. The user can choose from Reed and Form C relays; optically isolated inputs; and TTL, A/D, and D/A options. Available in bright, AMTFT LCDs ranging from 6.4 to 17 in., SeaPAC systems cost $1795.
Sealevel Systems, www.sealevel.com

VXS-processor mesh chassis provides high bandwidth

Available in 9 and 12U heights in various configurations, the VXS processor with a 12-slot mesh chassis provides a bandwidth of 112.5 Gbps of aggregate throughput within the processing mesh. This architecture includes a backplane feature combining VXS mesh slots, VXS payload slots, central I/O, and legacy VME64x slots. The VXS-processor mesh chassis costs $5000.
Elma Electronics, www.elma.com

VMEbus blade combines Intel hub and processor

The server-class-manageable Pentxm2 VMEbus blade combines the low-power, 1.67-GHz Intel dual-core Xeon processor and the Intel E7520 server-class MCH (memory-controller hub). The device provides a dual SATA-150, a triple USB 2.0 port, and an EIDE interface for an onboard disk or compact-flash support. Available with as much as 4 Gbytes of DDR2-400 SDRAM, the Pentxm2 costs $3950.
Thales, www.thalescomputers.com

Miniature motherboard has advanced audio/video capabilities

Expanding on the Procelerant Endura family, the TP945GM Mini-ITXexpress motherboard features an

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productroundup

EMBEDDED SYSTEMS

Intel Core Duo processor providing performance enhancements and a reduction in power consumption over previous generations. The Mobile Intel 945GM Express chip set with an integrated 3-D-graphics engine based on Intel Graphics Media Accelerator 950 architecture and eight-channel, high-definition audio enable advanced audio/video capabilities. Measuring 170×170 mm, the TP945GM motherboard costs $274.

RadiSys, www.radisys.com

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EDITED BY RON WILSON

scope

CHART YOUR COURSE

LOOKING AHEAD

ARM Developers' Conference

Ray Kurzweil will headline the ARM (www.arm.com) Developers' Conference, which will take place Oct 3 through 5 at the Santa Clara, CA, Convention Center. Kurzweil, one of the leading inventors of our time, will present his views on the acceleration of technology in the 21st century and its impact on business, the economy, and society. Conference-paper sessions and tutorial topics will include creating awesome multimedia, ARM on TV, memory-design tactics, virtualization, enhanced power management, microcontroller designs, overcoming multicore challenges, bus and system integration, and software-development strategies.

LOOKING BACK

50 YEARS AGO IN *EDN*

Where was that remote?

A new remote tuner that you can activate and control from anywhere in the room, or from an adjoining room, provides a means for silencing annoying TV commercials. Operating without wires, batteries, electricity, light, or radio waves, the unit also changes stations and turns the set on and off. You can carry the 8-oz control, "Space Command TV" from Zenith Radio Corp, anywhere in the room or house, and it is ready to do your bidding at the push of a button or the drop of a nerve-jangling sales slogan. The unit can kill commercials from anywhere within a home, but the device offers no help for interference from open windows or noisy neighbors.

–September 1956

LOOKING AROUND

A skeptical look at that notebook PC

Following last month's massive computer recalls to recapture possibly defective Sony lithium-ion batteries, it seems wise to give another suspicious glance to that notebook quietly charging on your desk. Scientists have known about the fire and explosion potential of lithium batteries since their earliest use in emergency-beacon equipment, but we have always convinced ourselves that proper handling, intelligent battery-control circuits, and good luck would prevent a problem. Since recent disclosures of serious fires on commercial aircraft, offices, and a battery vendor's plant, we may have to admit that we've been whistling past the graveyard. If batteries from first-tier companies can be dangerous, what about all the counterfeits that are probably out there?

Chipcon ZigBee™/ IEEE 802.15.4 Transciever

The CC2420 from Chipcon was the industry's first single-chip 2.4 GHz IEEE 802.15.4 compliant and ZigBee-ready RF transceiver. Chipcon's goal is to become the leading provider of this technology.

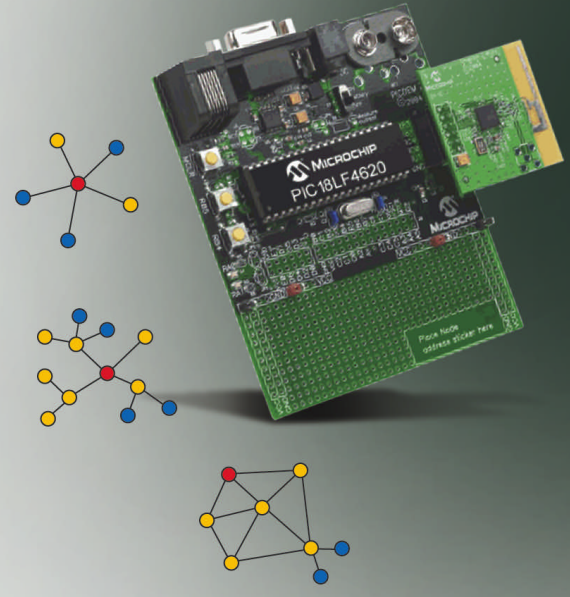
Chipcon Products from Texas Instruments mouser.com/chipcon/a

Helicomm 2.4 GHz ZigBee™ Embedded\OEM Modules

These IP-Link modules simplify wireless integration and reduce development cycles by six months or more. Each module includes an IEEE 802.15.4-compliant radio, a Silicon Laboratories 8051 microcontroller, programmable I/O, flexible antenna and range solutions, as well as ZigBee-ready IP-Net networking software.

Helicomm mouser.com/helicomm/a

Turn to Mouser for All Your ZigBee™ Product Needs!



Mouser delivers the newest products and the latest technologies, including ZigBee -- the hottest wireless technology protocol in the marketplace today.

Based on the IEEE 802.15.4, ZigBee is an open standard for reliable, cost-effective, low-power wireless applications. And it's a standard that works globally and can be configured for star, peer-to-peer, and mesh networks.

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Silicon Laboratories 2.4 GHz ZigBee™ Development Kit

Everything you need to immediately begin developing Star, Cluster-Tree, and Mesh Networks. Each of the six development boards included in the kit contains a high-performance C8051F121 MCU, an IEEE 802.15.4 compliant RF transceiver, the MAC firmware, and the Helimcomm ZigBee Protocol stack.

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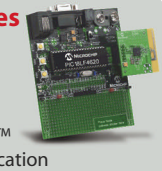
Microchip Technologies PICDEM™ Z Demonstration Kit



This kit is an easy-to-use ZigBee™ Technology wireless communication protocol development and demonstration platform. The kit includes the ZigBee protocol stack and two PICDEM Z boards, each with an RF daughter card. The demonstration board is also equipped with a 6-pin modular connector to interface directly with Microchip Technologies' MPLAB® ICD 2 in-circuit debugger (DV164005).

MICROCHIP mouser.com/microchip/a

Freescale ZigBee™ Evaluation Kits

Short range, low power, 2.4 GHz ISM band transceiver. Contains complete 802.15.4 PHY/MAC, ZigBee protocol stack supporting star, and mesh networking. The MC13193 can be a stand-alone transceiver or part of the Freescale ZigBee-ready platform when combined with an appropriate microcontroller.

freescale™ semiconductor mouser.com/freescale/a

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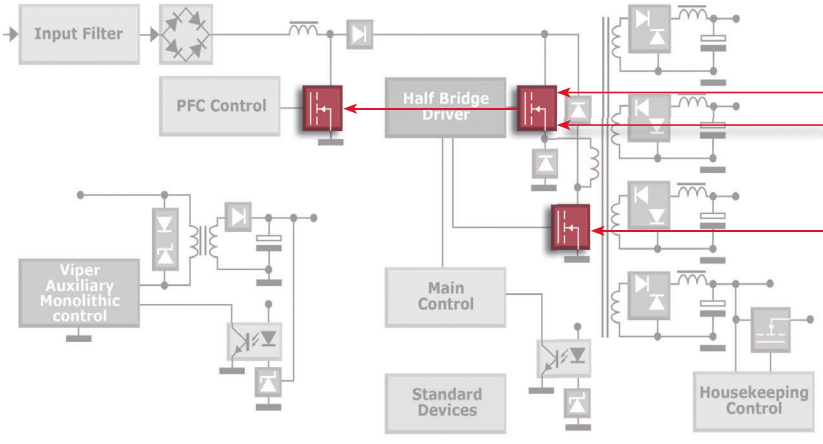
Solutions

MDmeshII Power MOSFETs with super-low $R_{DS(on)}$ give even lower power losses and easier driving for all your high-frequency SMPS applications.

Innovative products for multi-segment application systems



With ST's global solutions offerings such as Power Management ICs, Switching and Low Drop Regulator ICs and a wide range of advanced discrete devices, designing an SMPS for your application is easier than ever. The STP25NM60N using ST's unique MDmeshII™ technology, for example, offers one of the industry's lowest $R_{DS(on)}$ and new levels of performance at high frequencies.

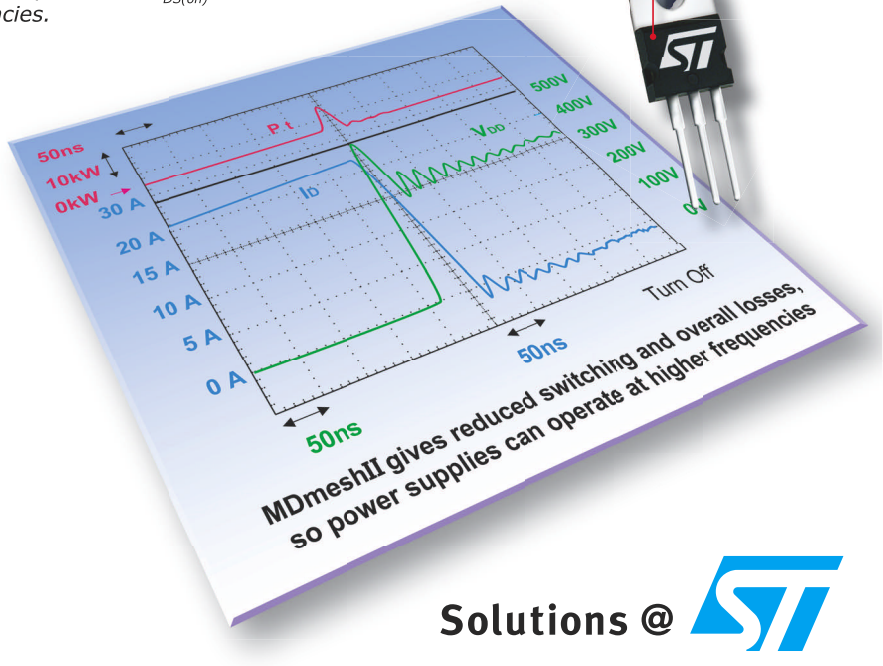
Key Features

- Up to 40% on-resistance reduction
- Typical $R_{DS(on)}$ = 0.140Ω
- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Part Number	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D	Pkge.
STB25NM60N-1	650V	< 0.170Ω	20A	I²PAK
STF25NM60N	650V	< 0.170Ω	20A*	TO-220FP
STP25NM60N	650V	< 0.170Ω	20A	TO-220
STW25NM60N	650V	< 0.170Ω	20A	TO-247
STB25NM60N	650V	< 0.170Ω	20A	D²PAK

* Limited only by maximum temperature allowed

For datasheets, application notes and more information visit
www.st.com/mdmesh



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